N° d'ordre: 2016LYSEC59
Année: 2016

THESE de DOCTORAT

DE L'UNIVERSITE DE LYON

opérée au sein de l'Institut des Nanotechnologies de Lyon (INL) à l'Ecole Centrale de Lyon

Ecole Doctorale: EEA-Electronique, Electrotechnique et Automatique

Spécialité: Electronique, micro et nano-électronique, optique et laser

Soutenue publiquement le 09/12/2016, par :

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Design Methods for Energy-Efficient Silicon Photonic Interconnects on Chip

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ACKNOWLEDGMENTS

This thesis has been a three-year work and exploring journey in the Institut des Nanotechnologies de Lyon (INL) at Ecole Centrale de Lyon in France, supported by China Scholarship Council. I am very grateful that in this period I have the chance to work with the professional and adorable researchers and friends. They contribute to this thesis in their own ways, to whom I would like to express my gratitude.

First of all, I must address my sincere gratitude to my PhD advisors Prof. Ian O’CONNOR and associate professor Sébastien LE BEUX for their great supervision and professional guidance through this three-year “adventure” of research.

I thank Ian for accepting me as a PhD candidate to work in his research team. I am grateful to do the research together with him. During the discussions with him, he can always open my vision and encourage me to keep moving, with his wide knowledge, his wisdom, his foresight, his calm, and his patience. I really appreciate his time, advises, and effort to make sure this thesis goes well and keep it on the right track.

At the same time, I thank Sébastien for contributing a huge effort to this thesis. He led me to learn more in different aspects on the research road, which helped me to find the direction and build my volition. Throughout this time, his intelligence, his organizing ability, his working efficiency, his good method, and his hard working motivated me all the time to carry forward. He always encouraged me to think creatively about the solutions and gave me a different angle to consider the work. He always pointed out the improvement space to approach the perfection. He discussed with me at both general view and the details, which was impressive, inspiring and helpful, even if sometimes it took time to agree with each other. He was supportive for me to attend the conferences to communicate with other researchers. When I encounter the issues, I could rely on receiving his comments/suggestions. I truly address my gratitude to him.

This thesis is related to multiple disciplines. The work would not have been possible without the help of Gabriela NICOLESCU and Alain FOURMIGUE from Ecole Polytechnique de Montréal, who provided us the thermal tool and relevant support on the thermal simulation. Xavier LETARTRE from INL, who contributed on the laser model, was another important person, providing us the solid device basis. Yvain THONNART (CEA - LETI / MINATEC,
Grenoble), our critical collaborator, contributed on the Microring Resonator model and helped validating the model in the work.

I would like to thank Prof. Lorena ANGHEL (TIMA-PHELMA, Grenoble) for accepting to be the president of the jury. In addition, I thank her for the comments on the work and the effort during the defense. I also thank Prof. David ATIENZA (ESL-EPFL, Lausanne) and Prof. Christophe PEUCHERET (FOTON-ENSSAT, Lannion) for accepting to be the external reviewers of my thesis and devoting their time/energy to the assessment. I also would like to address my thanks to Dr. Sébastien CREMER (STMicroelectronics, Crolles) and Yvain THONNART (CEA - LETI / MINATEC, Grenoble) for agreeing to be the examiners of my thesis and their efforts to examine the manuscript, as well as their detailed comments during the defense.

I address my thanks to Sylvie GONCALVES and Patricia DUFAUT for their administrative help. Sylvie was always patient and kind to me, and every time she could make things much more convenient for me, when I needed to deal with the registration and visa. I thank Laurent CARREL and Raphael LOPEZ who provided me technical help, and also David NAVARRO for reminding me on the thesis schedule. I discussed with Radoslaw MAZURCZYK on a number of interesting topics, exchanging various points of view.

I appreciate the time shared with my friends and the friendship with them. Zhen LI was the first PhD student that I knew even before coming to France. I appreciate the discussion with him. I enjoyed the time spent with Aleksandra PAVLOVA, with whom I shared a lot of common points. With Jean-Baptiste BARAKAT, Abdennacer BENALI, and Mateusz ZIELINSKI, we discussed a lot, and they helped me to know the lab better and also the culture of France. I am happy to have them as friends. I also thank Xiaopeng FU, Yong WU, and Yunnan GUO for accompanying me at the start of the life in France. I thank Xuchen LIU, Huanhuan LIU, He DING, Qiang LIU, Zhen LEI, and Liu SHI for helping me with the integration into France. I thank David ALLIOUX and Mihai APREUTESEI for the discussions. I truly appreciate to have the friendship with Marco VETTORI, with whom I discussed lots of interesting topics and who was always supportive and helpful. I thank Xin GUAN and Muchen LI for helping with the “pot”, which I appreciate so much. I also had pleasure of sharing time with Marie MINVIELLE, Mathieu CAILLAUX, Duc Kien TRAN, Ruping CAO, Rahma MOALLA, Malik KEMICHE, Florian DUBOIS, Jordan BOUAZIZ, Yue MA, Jian ZHANG, Benjamin MEUNIER, Daniel
THOMAS, Francois CHANCEREL, Louise FOUQUAT, Paul, Martha Johanna, and Martha Boeglin.

Finally, I would like to thank my family and my boyfriend for their constant love, support, and accompanying, and for the “shoulder” to cry on when I was going through the most stressful time. They are always there for me when I need. I dedicate this work to them. All in all, these three years are filled with happiness, tears, excitement, stress, and surprise. I appreciate every moment in this experience.
RESUME

La photonique au silicium est une technologie émergente considérée comme l'une des solutions clés pour les interconnexions sur puce de génération future, offrant plusieurs avantages potentiels tels qu'une faible latence de transmission et une bande passante élevée. Cependant, elle reste confrontée à des défis en matière d'efficacité énergétique. Différentes topologies, layout et architectures offrent diverses options d'interconnexion. Ceci conduit à une grande variation des pertes optiques, qui est l'un des facteurs prédominants dans la consommation d'énergie. De plus, les composants photoniques au silicium sont très sensibles aux variations de température. Sous une activité de puces donnée, ceci conduit à une réduction de l'efficacité des lasers et à une dérive des longueurs d'onde des composants optiques, ce qui entraîne un «Bit Error Ratio (BER)» plus élevé et réduit par conséquent l'efficacité énergétique des interconnexions optiques. Dans cette thèse, nous travaillons sur des méthodologies de conception pour les interconnexions photoniques sur silicium économiques en énergie et prenant en compte la topologie / le layout, la variation thermique et l'architecture.

Mots clés: méthodologie de conception, interconnexions photonique au silicium, topologie/layout, variation thermique, architecture, exploration
ABSTRACT

Silicon photonics is an emerging technology considered as one of the key solutions for future generation on-chip interconnects, providing several prospective advantages such as low transmission latency and high bandwidth. However, it still encounters challenges in energy efficiency. Different topologies, physical layouts, and architectures provide various interconnect options for on-chip communication. This leads to a large variation in optical losses, which is one of the predominant factors in power consumption. In addition, silicon photonic devices are highly sensitive to temperature variation. Under a given chip activity, this leads to a lower laser efficiency and a drift of wavelengths of optical devices (on-chip lasers and microring resonators (MRs)), which in turn results in a higher Bit Error Ratio (BER) and consequently reduces the energy efficiency of optical interconnects. In this thesis, we work on design methodologies for energy-efficient silicon photonic interconnects on chip related to topology/layout, thermal variation, and architecture.

Keywords: design methodology, silicon photonic interconnects, topology/layout, thermal variation, architecture, exploration
RESUME FRANCAIS

1. Introduction

D’après la loi de Moore, le nombre des transistors sur une surface de circuit intégré (IC) double tous les 18 mois. À mesure que la taille des transistors diminue, les performances augmentent [1] mais un mur de puissance apparaît. La limitation est due à la forte augmentation de densité sur une puce, proportionnellement à la vitesse à atteindre. Afin de permettre l’augmentation des performances, les concepts de circuits se sont dirigés vers les architectures multiprocesseurs [2].

Cependant, les performances globales et l'efficacité énergétique ne peuvent pas être améliorées correctement en raison des interconnexions électriques [3], qui souffrent d’un couplage capacitif et inductif, de résistance parasite, de bruit d'interconnexion et d’un délai propagation élevés. En particulier, les fils longs ne sont pas avantageux pour les interconnexions sur une puce car ils ont besoin de répéteurs tous les 1 mm ou moins pour maintenir la qualité du signal [4]. En outre, le budget de puissance de la communication inter-cœur exige une amélioration. Par exemple, environ 80% du budget total de la puissance est nécessaire pour les interconnexions métalliques au nœud technologique de 32 nm [5]. Dans l'ensemble, étant donné le nombre croissant de cœurs, des défis existent dans la conception de systèmes multi-cœur/many-cœur qui utilisent une interconnexion électrique traditionnelle [3].

La technologie de silicium photonique utilise le silicium comme milieu optique. La maturité de la transformation du silicium dans l'industrie CMOS donne la possibilité de fabrication à faible coût et à grande échelle [6]. En outre, le silicium peut fournir une transmission transparente à la longueur d'onde de télécommunication standard, par exemple, λ = 1550 nm. Il est également possible d'intégrer d'autres matériaux pour améliorer les fonctionnalités, comme le nitrure de silicium, les composés semi-conducteurs III-V, les éléments du groupe IV et ainsi de suite. Bénéficiant de la propriété avancée, les interconnexions photoniques au silicium sont prometteuses pour l'architecture de communication dans une variété d'applications, y compris les systèmes sur puce.

Le photonique silicium est un remplaçant potentiel de l’interconnexion électrique traditionnelle, tout comme la fibre optique a révolutionné l'industrie des télécommunications en
accélérant la transmission de l'information. Les interconnexions photoniques sur silicium utilisent des supports optiques pour transférer des données. C'est une technologie prometteuse et révolutionnaire qui présente des avantages en termes de la vitesse de transmission, de la largeur de bande agrégée et de l'efficacité énergétique par rapport aux interconnexions électriques traditionnelles.

Un avantage important des interconnexions photoniques sur silicium est la capacité d'utiliser le multiplexage par répartition en longueur d'onde (WDM), c'est-à-dire de fournir des canaux de longueur d'onde parallèles en utilisant différentes longueurs d'onde de lumière. Cette propriété offre une bande passante et une performance élevées. Ainsi, au lieu de liens optiques physiques parallèles, la technologie WDM offre un moyen rentable d'augmenter la bande passante en utilisant plusieurs longueurs d'onde. En outre, les interconnexions photoniques au silicium sont également avantageuses en termes d'évolutivité, de communication multicast et de reconfigurabilité.

Cependant, en raison des limitations technologiques, les interconnexions photoniques sur silicium rencontrent encore des défis [7][8] de fabrication, d'intégration optoélectronique, de fiabilité, d'efficacité énergétique et conception automatisé. Dans cette thèse, nous adressons la problématique des méthodologies de conception pour les interconnexions photoniques sur silicium efficace énergétiquement. Nous adressons les verrous suivants:

- **Topologie / layout**: Différentes topologies et configurations physiques offrent diverses options d'interconnexion pour la communication sur puce. Ceci conduit à une grande variation des pertes optiques. Une topologie ou un layout optimisé permet de réduire la consommation d'énergie de la source laser. Ainsi, l'exploration de l'espace de conception est nécessaire pour améliorer l'efficacité énergétique.

- **Variation thermique**: En raison de la répartition inégale de la consommation d'énergie sur la puce et de la sensibilité thermique des dispositifs photoniques, la variation thermique existe dans les interconnexions photoniques sur silicium sur puce. Cela a un impact significatif sur la fiabilité des communications et sur l'efficacité énergétique. Afin d'atténuer l'influence de la variation thermique, une solution est nécessaire qui est capable d'améliorer l'efficacité énergétique et de maintenir la fiabilité de la communication entre-temps.
- **Architecture**: Les schémas de communication et les affectations de ressources conduisent à des chemins de routage différents entre les sources et les destinations, ce qui contribue différemment à l'efficacité énergétique globale. Par conséquent, une architecture avec un schéma de communication optimisé est nécessaire.

Les principales parties de la thèse sont organisées comme suit:

Le chapitre 2 donne un aperçu de l'état de l'art des interconnexions photoniques au silicium sur puce. Après une introduction des technologies d'interconnexions photoniques au silicium sur puce, nous passons en revue les dispositifs optiques; puis, outre les architectures proposées, nous présentons deux variantes, la variation du processus et la variation thermique. Après un résumé des plates-formes de modélisation et de simulation existantes, nous mettons en évidence les principaux défis à relever dans cette thèse.

Le chapitre 3 explore les interconnexions photoniques au silicium sur puce avec diverses topologies et layouts physiques pour fournir des directives de conception. Ce chapitre étudie les topologies populaires, y compris les crossbars Matrix, λ-router, Snake, et ring. Il propose ensuite des layouts physiques pour les implémentations monocouche et multicouche. Il s’achève avec un modèle de pertes pour évaluer la perte optique la plus défavorable.

Le chapitre 4 propose une méthodologie de conception thermique afin d'améliorer l'efficacité énergétique tout en répondant aux exigences de fiabilité des communications. Ce chapitre commence par l'analyse de l'influence de la variation thermique des interconnexions photoniques au silicium sur puce. Il se poursuit par une présentation de la méthodologie de conception thermique proposée. Il se termine avec le modèle de transmission, le modèle de puissance et le modèle de simulation, afin d'évaluer la fiabilité et l'efficacité énergétique des interconnexions optiques.

Le chapitre 5 propose un réseau optique sur puce, appelé CHAMELEON. Cette architecture peut améliorer l'efficacité énergétique et l'utilisation des interconnexions optiques en configurant de manière flexible l'interconnexion optique entre les sources et les destinations. Ce chapitre commence par une introduction de l'architecture réseau; s’ensuit une présentation des méthodes de configuration, y compris les applications mappées au moment de la conception et le protocole de communication au moment de l'exécution. Enfin, il évalue l'efficacité énergétique de l'architecture proposée.
Le chapitre 6 conclut la thèse et discute du travail en perspective dans le domaine des interconnexions photoniques au silicium.

2. Etat de l'art des interconnexions photoniques au silicium sur puce

Les interconnexions photoniques sur silicium sur puce ont le potentiel de fournir des propriétés supérieures de faible latence, de bande passante élevée et de faible consommation d'énergie [9], par rapport aux interconnexions électriques traditionnelles. Comme représentés sur la Figure 1, les interconnexions sont fondamentalement composées de dispositifs optiques tels que des sources laser, des guides d'ondes, des résonateurs à microring (MRs) et des photodétecteurs.

Figure 1: Vue générale des interconnexions photoniques silicium sur puce en méthode de modulation indirecte [10].

Des sources laser (par exemple, Figure 2) sont utilisées pour émettre des signaux optiques.

Figure 2: Vue 3D de PCM-VCSEL [21].
Les signaux optiques sont modulés (par exemple, un modulateur est représenté sur la Figure 3) en mode direct (c'est-à-dire modulation au niveau des sources laser) ou indirect (c'est-à-dire au niveau des modulateurs). Par exemple, chaque bit de données "1" ou "0" peut être représenté par la présence ou l'absence de la porteuse dans la modulation de "on-off keying" (OOK).

Figure 3: a) Disposition schématique du modulateur à base de MR; b) la mesure de DC du MR, avec les spectres de transmission du MR à différentes tensions de polarisation (par exemple, 0,58 V, 0,87 V et 0,94 V, respectivement). L'encart montre la fonction de transfert du modulateur pour la lumière avec une longueur d'onde de 1573,9nm [1]. (Les figures sont extraites de la réf. [11])

Après la modulation, des signaux optiques transmettent dans des guides d'ondes (par exemple, représentés sur la Figure 4) de la source à la destination.

Figure 4: Structure transversale d'un guide d'ondes photonique en silicium typique [12].
Du côté de la destination, les filtres optiques déposent les signaux optiques en photodétecteurs (par exemple, représentés sur la Figure 5), puis les photodétecteurs convertissent les signaux optiques en un domaine électrique.

![Photodétecteur Ge intégré sur un guide d'onde en silicium](image)

**Figure 5:** Photodétecteur Ge intégré sur un guide d'onde en silicium [13].

### 3. Lignes directrices de topologie passive et layout

La diminution de la perte pire cas est obligatoire pour réduire la consommation d'énergie globale du système. Les principales sources de pertes sont composées de la propagation du signal dans les guides d'onde, les croisements de guides d'onde et la couplage de MR. La réduction des pertes peut être obtenue par: i) l'amélioration de la topologie du réseau; ii) l'optimisation du layout; et iii) l'utilisation d'un nouveau procédé de fabrication tel que la technologie multicouches déposée au silicium.

De nombreuses interconnexions photoniques sur silicium reposant sur WDM ont été proposées. En outre, le schéma de routage de longueur d'onde peut être utilisé pour propager des données d'un cœur IP source vers un cœur IP destination, conduisant à un réseau sans contention, appelé WRONoC (c'est-à-dire ONoC acheminé en longueur d'onde).

Les topologies transversales considérées dans ce travail sont: Matrice [14], λ-routeur [15], Snake [16] et ORNoC [17], comme montré dans la Figure 6. Dans la figure, chaque colonne est dédiée à une topologie et les lignes montrent leurs i) vues structurelles et ii) caractéristiques de mise en œuvre. Nous présentons brièvement ces topologies et illustrons la façon dont elles peuvent être utilisées pour interconnecter des 2×2 IP cœurs. Nous évaluons également le nombre de dispositifs optiques requis, en supposant que \( N \) est un nombre pair. \( N_{\text{MR}}, N_{\text{MR, det}}, N_{\text{laser}} \) et \( N_{\text{wl}} \), représentent le nombre de MRs dans le réseau lui-même après la réduction, le nombre de MRs
dans l'interface du récepteur, le nombre de sources laser et le nombre de longueurs d'onde. Dans ce travail, nous considérons des crossbars optiques complètement reliées.

<table>
<thead>
<tr>
<th>Structural view</th>
<th>a) Matrix</th>
<th>b) λ-router</th>
<th>c) Snake</th>
<th>d1) ORNoC_{C}</th>
<th>d2) ORNoC_{C,CC}</th>
</tr>
</thead>
<tbody>
<tr>
<td>( N_{MR} )</td>
<td>((N^2 - 1) \times N^2)</td>
<td>((N^2 - 2) \times N^2)</td>
<td>((N^2 - 2) \times N^2)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>( N_{MR,\text{det}} )</td>
<td>((N^2 - 1) \times N^2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( N_{\text{laser}} )</td>
<td>((N^2 - 1) \times N^2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( N_{\text{wl}} )</td>
<td>(N^2 - 1)</td>
<td>(N^2)</td>
<td>(N^2)</td>
<td>((N^2 - 1) \times N^2 / 2)</td>
<td>((N^2 - 1) \times N^2 / 4)</td>
</tr>
</tbody>
</table>

Figure 6: Crossbars optiques: a) Matrix, b) λ-router, c) Snake, d1) ORNoC_{C} and d2) ORNoC_{C,CC}.

**Layout monocouche**

La Figure 7 illustre le modèle d'architecture 3D considéré. Il se compose d'une couche électrique et d'une couche optique. La couche électrique est composée de cœurs IP qui sont uniformément disposés en un maillage \(N \times N\), \(N\) étant égal à un nombre pair (par exemple \(N = 4\) sur la Figure 7). Les IP cœurs traitent et stockent des données, et les données entre les cœurs sont échangées par une traverse optique mise en œuvre en utilisant la couche optique (topologie en anneau dans l'exemple). La couche optique est composée de dispositifs optiques, tels que des lasers à puce (par exemple VCSEL [18]), des guides d'ondes, des MRs et des photodétecteurs. Les deux couches sont connectées en utilisant TSV [19]. Dans notre travail, nous supposons que \(N\) est un nombre pair, mais le travail pourrait être facilement étendu pour les valeurs impaires et pour des architectures avec \(N \times M\) IP cœurs.
Figure 7: La optique (topologie en anneau dans l'exemple) est implémentée dans la couche optique et elle interconnecte des IP cœurs situés dans la couche électrique.

Pour les crossbars optique populaires, nous nommons les implémentations mono-couche correspondantes comme MatrixSL, λ-routerSL, SnakeSL, et ORNoCSL. Les sources laser sur puce sont préssumées pour toutes les configurations puisqu'elles ne conduisent pas à l'utilisation de guides d'ondes de puissance comme pour les lasers hors circuit, ce qui contribue à réduire le nombre de croisements de guide d'ondes et ainsi améliorer l'efficacité énergétique.

Figure 8: Résumé des crossbars optiques considérées: a) layout\textsuperscript{aX}\textsubscript{SL} et b) layout\textsuperscript{bX}\textsubscript{SL} pour MatrixSL, λ-routerSL, et SnakeSL, c1) ORNoC\textsuperscript{c}\textsubscript{SL}, et c2) ORNoC\textsuperscript{c,CC}\textsubscript{SL}.
Figure 8-a et -b présentent deux schémas possibles: i) layout\textsuperscript{w/oX} et ii) layout\textsuperscript{wX}, qui sont respectivement conçus pour i) éviter tout croisement de guide d'ondes entre les interfaces de réseau et le réseau de crossbars lui-même et ii) réduire la longueur du guide d'ondes la plus défavorable entre les IP cœurs.

**Layouts multi-couches**

Dans cette section, la technologie de silicium déposé multicouches est utilisée pour réduire la perte optique et ainsi améliorer l'efficacité énergétique. Nous nommons les layouts multi-couches correspondantes comme Matrix\textsubscript{ML}, λ-router\textsubscript{ML}, Snake\textsubscript{ML}, et ORNoC\textsubscript{ML}.

![Diagramme de Crossbar optique](image)

**Figure 9**: Crossbar optique (topologie en anneau dans l'exemple) est implémentée dans les couches optiques et elle interconnecte les IP cœurs.

La Figure 9 illustre le modèle d'architecture 3D considéré, en utilisant un exemple d'architecture pour les 4x4 IP cœurs. Différent de l'implémentation monocouche, deux couches optiques (topologie en anneau pour l'interconnexion optique dans l'exemple) sont utilisées et empilées sur une couche électrique.

La Figure 10-a illustre une mise en œuvre multicouche de Matrix utilisée pour interconnecter quatre cœurs. On évite le croisement de guides d'onde en allouant des guides d'ondes d'entrée et de sortie respectivement sur la première et la deuxième couche. Pour sa mise en œuvre, Matrix utilise 16 MRs pour interconnecter complètement les 4 cœurs. Les MRs situés sur la diagonale peuvent être supprimés si l'on considère uniquement les communications entre les cœurs, ce qui conduit à des \((N^2-1)\times N^2\) pour l'architecture \(N\times N\).
λ-router et Snake sont des réseaux optiques à plusieurs étages qui peuvent être mis en œuvre de manière similaire, comme illustré dans les Figure 11-a et -b. Les signaux optiques se propagent le long des guides d'onde et sont chassés d'un guide d'onde à un autre, afin d'atteindre les sorties ciblées. La structure de commutation de λ-router et Snake est un PSE symétrique mis en œuvre avec deux MRs identiques. La méthode proposée dans [15] est également utilisée: en ne gérant que les communications requises, les PSE inutiles sont supprimées, ce qui contribue à réduire la complexité du réseau. En considérant uniquement les communications inter-œuf, les PSE situés dans la rangée centrale et la colonne centrale de λ-router et Snake sont supprimés, respectivement.

Figure 10: a) Matrix_{ML} topologie, b) layout sans croisement de guides d'onde (layout_{ML}^{wX}) et c) layout avec la longueur de guide d'ondes la plus courte (layout_{ML}^{xX}).
Figure 11: a) λ-router\textsubscript{ML} et b) Snake\textsubscript{ML} et layouts c) sans croisement de guides d'onde (layout\textsuperscript{wX\textsubscript{ML}}) et d) avec la longueur de guide d'ondes la plus courte (layout\textsuperscript{wX\textsubscript{ML}}).

ORNoC est un crossbar optique à base d'anneau [17][20] illustrée sur le côté gauche de la Figure 12. La principale caractéristique de ORNoC est l'absence de croisements de guide d'ondes, ce qui est possible en raison de la disposition en serpentin et de l'utilisation des lasers à puce.
Dans la figure, les lignes pleines et les lignes à points représentent respectivement les directions dans le sens des aiguilles d'une montre (C) et dans le sens inverse des aiguilles d'une montre (CC). La même longueur d'onde peut être utilisée pour réaliser simultanément plusieurs communications dans le même guide d'ondes, mettant en œuvre efficacement le schéma de communication Single-Write-Single-Read (SWSR). Cela n'est possible que si les différentes communications n'ont pas de chemin de chevauchement. En outre, de multiples guides d'ondes peuvent être utilisés pour transmettre le signal optique dans les directions C et CC.

**Figure 12: Crossbars optiques ORNoC<sub>SL</sub> et ORNoC<sub>ML</sub>: a) topologie pour interconnecter 9 IP cœurs et b) layout pour 4 × 4 IP cœurs.**

ORNoC<sub>ML</sub> est l'implémentation multi-couches de ORNoC et est illustrée sur le côté droit de la Figure 12. Elle implémente un deuxième ensemble d'anneaux situés sur la deuxième couche, dans le but d'améliorer la connectivité entre les cœurs IP grâce à des pertes réduites. Les couleurs rouge et bleue sont utilisées pour représenter les guides d'onde situés respectivement dans la première et la deuxième couche. Les dispositions d'anneau dans la seconde couche sont tournées de 90 ° par rapport à la disposition de la première couche. Etant donné que les guides d'ondes
supplémentaires sont situés dans une couche différente, la propagation du signal ne souffre d'aucune perte de passage de guide d'ondes supplémentaire.

4. Méthodologie de conception thermique pour maximiser l'efficacité énergétique

Influence de la variation thermique dans les interconnexion photonique sur silicium

Les dispositifs photoniques au silicium sont très sensibles à la variation de température induite par l'effet thermique sur la puce, ce qui conduit à une dérive de la longueur d'onde du laser et de la longueur d'onde résonante des MRs le long d'un chemin de communication. En conséquence, le rapport signal sur bruit (SNR) des signaux reçus par le photodétecteur diminue, ce qui conduit à un taux d'erreur de bits (BER) plus élevé et à une efficacité énergétique inférieure (en raison de la retransmission). Ceci est encore accentué par la réduction significative de l'efficacité des lasers sur puce à mesure que la température augmente.

Nous supposons une architecture 3D similaire au chapitre 3, c'est-à-dire une couche optique au-dessus d'une couche électrique. Les ONIs sont constitués de lasers à puce et de MR, responsables de la modulation et de la réception du signal optique sur la couche optique.

Les lasers à puce (par exemple, les lasers à base de VCSEL [21][22]) fournissent la puissance optique par l'entraînement du courant. Alors que les procédés de fabrication des VCSEL compatibles CMOS sont moins matures que ceux des lasers microdisk [23], ils offrent un avantage significatif en termes d'évolutivité (une puissance de sortie laser plus élevée est réalisable et la disposition peut être plus souple) et la densité spectrale en raison de leur petite taille 3dB bande passante (typiquement 0.1nm). L'inconvénient des lasers à puce sur les contreparties hors-puce est leur efficacité intrinsèquement inférieure et une plus grande sensibilité à la variation de l'activité de la puce étant donné qu'elles sont situées au-dessus de la couche de traitement. Plus précisément, chaque laser à puce est situé au-dessus d'un pilote CMOS qui commande le courant laser (I\textsubscript{laser}), comme illustré sur la Figure 13-a. Le courant se propage via un TSV et pilote directement le laser sur puce. Un signal optique est émis verticalement et est redirigé vers un guide d'onde horizontal à travers un cône. La puissance optique injectée dans le réseau (OP\textsubscript{net}) dépend donc i) de l'intensité du courant laser I\textsubscript{laser}, ii) de l'efficacité du laser (\eta\textsubscript{laser}) et iii) de l'efficacité du couplage conique (\eta\textsubscript{coupling}, supposé être de 80%). Par exemple, une efficacité VCSEL est très sensible à sa température: il peut chuter de 15%
à 40°C à 4% à 60°C. Cette efficacité plutôt faible entraîne une puissance dissipée élevée ($P_{\text{laser}}$) qui, avec la puissance dissipée par le pilote CMOS ($P_{\text{driver}}$) et la partie de puce à la zone source/entourant ($P_{\text{chip}}$), influence la température laser sur puce. Ainsi, pour un courant donné, la puissance du signal optique émis ($OP_{\text{laser}}$) dépend de la température du laser, influencée par $P_{\text{chip}}$, $P_{\text{laser}}$ et $P_{\text{driver}}$, comme illustré sur la Figure 13-a. L'influence de la température laser sur la propagation du signal est illustrée à la Figure 13-b.

Figure 13: a) Communication générique dans les interconnexions photoniques au silicium, en tenant compte de l'effet thermique. L’efficacité d’un laser sur puce (par exemple, VCSEL) et de la longueur d'onde du signal émis dépend de sa température, qui est influencée par le pilote CMOS et l’activité de la puce. La longueur d'onde résonante MR dépend de la température de MR, qui est influencée par les lasers, l'activité des puces et la puissance de calibrage MR. b) Le signal à la modulation (La marque "\(\Phi\)" représente les données électriques avant modulation, et la marque "\(\Phi'\)" représente le signal optique après modulation); c) Le signal à la photodétection (La marque "\(\Phi\)" représente le signal optique avant photodétection, et la marque "\(\Phi'\)" représente les données électriques après photodétection).

Pendant ce temps, la longueur d'onde du signal émis est influencée par la température du laser. Idéalement, la longueur d'onde du laser est conçue pour être égale à la longueur d'onde résonante MR correspondante du côté cible, ainsi que les MR le long du trajet. Cependant, la longueur d'onde résonante MR peut également dériver avec sa température. Par exemple, la
température de la MR au photodétecteur est influencée par la puissance dissipée par la partie puce au niveau de la zone cible / entourant (P’_{chip}) et également le laser sur puce (P’_{laser}) (Figure 13-a). En résumé, la puissance du signal diminuée par le MR au niveau du côté cible (OP_{pd}) dépend également de l'alignement de la longueur d'onde parmi les dispositifs optiques, influencé par la température du gradient entre différentes interfaces, comme illustré sur la Figure 13-c. Ainsi, une température moyenne basse et une température de gradient sont nécessaires.

En outre, pour une activité croissante de la couche de traitement (qui devrait donner lieu à des communications additionnelles), soit la largeur de bande d'interconnexion optique diminuera en supposant un même courant laser (c'est-à-dire que le BER soit plus élevé, les données seront réémises) soit la consommation électrique d'interconnexion optique augmentera (c'est-à-dire qu'un courant laser plus élevé est nécessaire pour compenser une efficacité réduite). Le courant laser doit donc être soigneusement sélectionné car i) une valeur trop faible conduira à un BER élevé et ii) une valeur trop élevée conduira à une solution de faim de puissance.

En conclusion, les dispositifs optiques à base de silicium sont sensibles à la variation thermique (0.1nm/°C typiquement [24]), ce qui induit l'incompatibilité des longueurs d'onde des dispositifs photoniques au silicium le long d'un canal de communication. En conséquence, la puissance du signal optique reçue du côté du lecteur diminue, ce qui se traduit par un SNR inférieur et un BER plus élevé. En outre, l'efficacité des lasers sur puce est réduite lorsque la température augmente, c'est-à-dire que le BER est encore dégradé. Afin de traiter cette problématique, nous proposons une méthodologie de conception thermique pour assurer un BER ciblé côté lecteur tout en minimisant la consommation d'énergie.

**Méthodologie proposée**

Dans ce travail, nous présentons une méthodologie proposée permettant de concevoir une interconnexion photonique de silicium thermorésistant.

La méthodologie proposée (Figure 14) vise à parvenir à un compromis entre l'efficacité énergétique et la fiabilité, et permet d'explorer l'espace de conception au niveau du dispositif et du système. A cet effet, les caractéristiques principales des dispositifs optiques (par exemple, les lasers, les MRs, les guides d'onde, les photodétecteurs) sont prises en compte dans les modèles au niveau du dispositif. Les aspects architecturaux tels que la taille de l'interconnexion, la
topologie/layout, et les technologies d'implémentation sont pris en compte dans les modèles au niveau du système, comme le montrent les "Modèles IP" de la Figure 14.

Les paramètres d'entrée de clé au niveau de l'appareil (par exemple, le courant du pilote laser ($I_{\text{laser}}$) et la puissance de calibrage MR ($P_{\text{MR}}$)) et le niveau du système (par exemple, l'activité de la puce et le schéma de communication) sont spécifiés par les utilisateurs. $I_{\text{laser}}$ et $P_{\text{MR}}$ peuvent être réglés pour aligner les longueurs d'onde du laser et des MRs. Différentes activités de puces (par exemple, uniformes, diagonales et coin) simulent la puissance dissipée par la couche de traitement et le schéma de communication détermine les chemins de signal.

Sur la base d'un ensemble de paramètres d'entrée au niveau du périphérique et du système, la simulation thermique effectue une analyse thermique. Il permet l'estimation des profils de
température sur la puce, fournissant la température du gradient et la température moyenne des composants optiques. Dans notre méthodologie, la sensibilité thermique des sources laser sur puce est prise en compte. À partir des cartes de température générées, les modèles analytiques établis (c'est-à-dire le modèle de puissance et le modèle BER) permettent d'évaluer l'efficacité énergétique et la fiabilité des interconnexions optiques considérées, avec la consommation d'énergie de calibrage et le BER comme métriques. Les résultats de l'analyse de puissance et de l'analyse BER sont à la base de l'exploration et de l'optimisation de l'espace de conception.

Pour un paramètre d'entrée donné au niveau du système, les paramètres d'entrée au niveau du périphérique de calibrage (c'est-à-dire I_laser et P_MR) permettent d'explorer l'espace de conception au niveau du périphérique et du système, comme le montre la flèche rouge de la Figure 14. En attendant, cela permet un compromis entre l'efficacité énergétique et la fiabilité des interconnexions optiques. De plus, cette méthodologie est générique et peut être appliquée à l'analyse à la fois stationnaire et transitoire.

Basé sur la méthodologie, nous proposons une méthode de calibrage laser à puce thermique pour surmonter la variation de longueur d'onde induite par la variation de température, tout en réalisant le BER ciblé en attendant. La nouveauté de la méthode repose sur le calibrage du courant pilote du laser, qui complète idéalement les méthodes traditionnelles telles que le calibrage des MRs et le remappage des canaux [25][26]. Alors que le procédé est évalué pour des sources laser sur puce, il est également approprié pour les lasers hors-puce puisque l'impact d'une élévation de température resterait le même.

**Alignement des longueurs d'onde des signaux et des MRs**

La Figure 15 illustre notre méthode dans le contexte d'un canal MWSR [27] avec une seule source laser, 2 écrivains et un lecteur. Dans notre travail, nous considérons les lasers distribués qui sont situés dans la même couche avec MRs, guides d'onde et photodétecteurs. Pour cela, nous supposons l'utilisation de sources laser compatibles CMOS telles que VCSELs, dont la taille est similaire à celle des MRs. Comme illustré sur la Figure 15-a, ONI_m communique avec ONI_r: le MR dans l'ONI_i intermédiaire est mis à OFF tandis que le MR dans l'ONI_m est en état de modulation (état OFF et ON pour moduler respectivement les données «1» et «0»).
Figure 15: a) MWSR canal avec une longueur d'onde et deux écrivains, b) transmission sans variation thermique (cas idéal), c) transmission selon la seule méthode de calibrage MR avec des sources laser hors-puce, et d) transmission avec notre méthode de calibrage de laser sur puce proposée.

La Figure 15-b illustre la transmission idéale d'une donnée «1» qui se produit lorsqu'il n'y a pas de variation de température le long du trajet de communication. Le signal optique injecté par le laser (qui est caractérisé par une puissance $OP_{\text{ideal}}$ et une longueur d'onde $\lambda_{\text{laser}}$) croise ONI$_{\text{m}}$ et ONI$_{\text{i}}$, se propage le long du guide d'ondes jusqu'à ONI$_{\text{r}}$, où il est tombé au photodétecteur (comme illustré par les lignes de transmission bleues sur la Figure 15-b). La puissance du signal optique diminue le long du trajet en raison des pertes de propagation du guide d'onde et des MRs traversant les pertes (ligne bleue de la Figure 15-b). Le BER est estimé sur la base de la puissance optique reçue $OP_{\text{pd,ideal}}$, de la sensibilité du récepteur et de la diaphonie (induite par d'autres signaux de transmission à différentes longueurs d'onde, non illustrées par souci de clarté mais prises en compte dans nos modèles).

**Méthode de calibrage MR seule**

En cas de gradient de température sur le trajet de communication, la longueur d'onde résonante des MRs dérivera (voir les lignes de transmission rouge sur la Figure 15-c) tandis que la longueur d'onde du signal émis ($\lambda_{\text{laser}}$) reste la même au cas où les lasers hors circuit sont pris en considération. Sans compenser l'effet de cette dérive, le désalignement entre la longueur d'onde du signal et les longueurs d'onde résonnantes de MRs conduit à un BER sensiblement augmenté. Pour surmonter cet effet, les MRs le long du guide d'ondes sont accordés à leurs positions initiales (les lignes de transmission grises de la Figure 15-c) en utilisant un accord
thermique ou un calibrage de tension. La transmission du signal de post-accord est illustrée par la ligne bleue de la Figure 15-c: la puissance optique reçue est légèrement inférieure à celle dans le scénario idéal en raison du désalignement des longueurs d'onde marginales. La puissance de calibrage des MR dépend de leur dérive de température ($\Delta T_{MR,m}$, $\Delta T_{MR,i}$ et $\Delta T_{MR,r}$) et du coefficient de sensibilité thermique $\rho_{MR}$. La consommation d'énergie totale du canal est donnée par la somme de la consommation de puissance du laser $P_{laser}$ et de la puissance de calibrage MRs $\sum P_{MR}$.

**Méthode de calibrage proposée de laser et MR**

La nouveauté clé de notre méthode repose sur le calibrage du courant de polarisation laser: puisque la température laser varie avec son courant de polarisation, la longueur d'onde du signal optique peut être réglée. Par conséquent, en plus d'accorder les MR pour aligner les longueurs d'onde résonnantes avec le signal optique, nous accordons également la longueur d'onde du signal optique lui-même, ce qui contribue à réduire la puissance requise pour compenser la variation thermique.

Comme l'illustre dans la Figure 15-d, le calibrage du courant de commande $I_{laser}$ a un impact sur la consommation d'énergie du laser et sur la longueur d'onde du signal émis: celui-ci varie de $P_{laser}$ à $P'_{laser}$ et celui-ci passe de $\lambda_{laser}$ à $\lambda'_{laser}$. Par conséquent, sous le même gradient de température considéré dans la Figure 15-c, les longueurs d'onde des MR doivent être accordées à $\lambda'_{laser}$, au lieu de $\lambda_{laser}$ (voir les lignes de transmission vertes sur la Figure 15-d). La puissance de calibrage des MR diminue puisque la distance des longueurs d'onde est réduite. Comme inconvénient, la puissance du signal émis est réduite, ce qui signifie qu'un compromis doit être défini pour atteindre le BER cible tout en diminuant la consommation totale du canal. Il est intéressant de noter que, bien que le procédé soit illustré avec un canal à 1 longueur d'onde, il est générique et il peut être appliqué aux canaux WDM, comme illustré dans la section des résultats. De plus, il est complémentaire à des méthodes associées fournissant un remappage de canal [25][26] que nous avons adapté pour minimiser la puissance de calibrage au lieu de la distance de calibrage.

5. **CHAMELEON: CHANNEL Efficient Optical Network-on-Chip**

Dans le chapitre 3, nous avons exploré plusieurs topologies et constaté que la topologie en anneau montre une plus grande efficacité énergétique en prenant en considération la perte le pire-
cas. De plus, la combinaison des sens de communication dans le sens des aiguilles d'une montre (C) et dans le sens inverse des aiguilles d'une montre (CC) permet de réduire davantage la perte du pire cas et d'améliorer ensuite l'efficacité énergétique. Pour faire bon usage de ces bonnes propriétés, une solution est considérée dans le point de vue de l'architecture.

Dans ce chapitre, nous proposons CHAMELEON, qui signifie CHANNEL Efficient ONoc, un réseau optique reconfigurable sur puce (ONoC). La reconfiguration de CHAMELEON peut être spécifiée au moment du design en utilisant la méthode de cartographie statique, ou obtenue au moment de l'exécution via un protocole de communication. Les caractéristiques principales de l'architecture proposée sont les suivantes: tout d'abord, CHAMELEON étend l'approche SWSR (c'est-à-dire ORNoC, précédemment décrite au chapitre 3) avec une fonctionnalité de reconfigurabilité permettant l'ouverture et la fermeture de canaux dédiés entre les cœurs IP. Par conséquent, la bande passante du réseau est hautement adaptable en fonction des exigences de communication. Deuxièmement, la même longueur d'onde peut être utilisée sur des parties de guide d'ondes qui ne se chevauchent pas, conduisant ainsi à un réseau fortement utilisé et à une plus grande bande passante en considérant le partitionnement de guides d'ondes. Troisièmement, grâce à l'utilisation combinée de lasers à puce et à la fois dans le sens horaire et dans le sens inverse des aiguilles d'une montre pour la propagation du signal, la consommation d'énergie peut être réduite. Enfin, une plus grande évolutivité et une synthèse du layout facile sont obtenues grâce aux ONIs régulières et à la topologie en anneau.

CHAMELEON est implanté dans une couche optique, au sommet d'une couche électrique mettant en œuvre des cœurs IP, similaire à l'architecture 3D présentée au chapitre 3. La topologie et la disposition sont semblables à des serpentins, semblables à ORNoC [17]. CHAMELEON permet également la réutilisation de longueurs d'onde pour réaliser plusieurs communications indépendantes dans un seul guide d'ondes en considérant le cloisonnement de guide d'onde.

Systèmes de communication

CHAMELEON est capable de réaliser de multiples schémas de communication grâce à la reconfigurabilité, comme illustré à la Figure 16.
Figure 16: Possibilités de communication: a) SWSR, b) SWMR, c) MWSR, et d) Canal à large bande passante.

- **SWSR (Single Writer Single Reader, i.e., des canaux de communication point à point dédiés),** est facilitée par le partitionnement du guide d'ondes, ce qui permet de réutiliser une longueur d'onde donnée pour réaliser plusieurs communications indépendantes dans le même guide d'onde. Sur la Figure 16-a, $\lambda_0$ est utilisé pour réaliser des communications $\text{ONI}_A \rightarrow \text{ONI}_B$, $\text{ONI}_B \rightarrow \text{ONI}_C$ et $\text{ONI}_C \rightarrow \text{ONI}_A$. Concrètement, $\lambda_1$ et $\lambda_2$ sont utilisés pour réaliser respectivement $\text{ONI}_C \rightarrow \text{ONI}_B$ et $\text{ONI}_A \rightarrow \text{ONI}_D$. Ceci facilite le partitionnement virtuel d'un guide d'ondes pour une longueur d'onde donnée.

- **SWMR (Single Writer Multiple Readers, i.e., diffusion / multidiffusion)** peut être réalisée en ouvrant des canaux de communication dédiés entre une source ONI et toutes les ONIs restantes (respectivement les ONIs de destination). Sur la Figure 16-b, $\text{ONI}_B$ diffuse des données à $\text{ONI}_C$, $\text{ONI}_D$ et $\text{ONI}_A$ par des longueurs d'onde $\lambda_0$, $\lambda_1$ et $\lambda_2$ respectivement.

- **MWSR (Multiple Writers Single Reader)** peut être réalisée en ouvrant des canaux de communication entre plusieurs ONI sources et une destination ONI identifiée. Sur la Figure 16-c, $\text{ONI}_A$, $\text{ONI}_B$, et $\text{ONI}_C$ envoient respectivement des données à $\lambda_0$, $\lambda_1$ et $\lambda_2$ à l'interface de destination $\text{ONI}_D$. 

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**Figure 16:** Possibilités de communication: a) SWSR, b) SWMR, c) MWSR, et d) Canal à large bande passante.
En outre, des canaux à large bande passante peuvent être ouverts en allouant plusieurs longueurs d'onde pour une communication donnée. Ceci est adapté à l'exécution d'applications de streaming qui nécessitent le transfert d'une grande quantité de données d'un cœur IP vers un autre. Dans la Figure 16-d, les canaux de communication à large bande passante sont ouverts de l'ONI_B à l'ONI_D et de l'ONI_D à l'ONI_A.

Ces schémas de communication peuvent être combinés tant qu'une largeur de bande suffisante dans le réseau est disponible. Par exemple, des canaux de largeur de bande élevée peuvent être ouverts, tandis que d'autres canaux de bande passante inférieure sont déjà ouverts. Cette grande flexibilité permet à CHAMELEON d'exécuter des applications dans différentes classes. Cependant, l'ouverture des canaux à la granularité de la longueur d'onde conduit à une plus grande complexité du réseau de contrôle, ce qui peut entraîner une latence supplémentaire pendant l'allocation des ressources optiques aux canaux. Pour rendre CHAMELEON efficace, chaque canal devrait ainsi transmettre un ensemble de données aussi important que possible avant sa fermeture. Cela convient particulièrement bien au modèle de streaming de calcul, car il nécessite habituellement le transfert d'une grande quantité de données pendant une courte période. De plus, puisque CHAMELEON permet de combiner différents canaux en une seule configuration en même temps, un degré de flexibilité / réutilisation élevé est atteint.

Figure 17: Canaux de communication bidirectionnels. Les couleurs bleue et rouge représentent respectivement les directions C et CC.
Les schémas de communication de la Figure 16 sont illustrés en utilisant un guide d'ondes, ce qui signifie qu'une seule direction de communication est disponible, par exemple, dans le sens des aiguilles d'une montre (C) sur la figure. En fait, de multiples guides d'ondes peuvent être utilisés pour propager des signaux optiques dans les deux directions (C) et anti-horaire (CC), comme illustré sur la Figure 17. En plus de réduire les pertes les plus défavorables du réseau (par conséquent, la consommation d'énergie, comme cela sera discutée plus loin), cela permet l'ouverture de canaux de communication dédiés bidirectionnels, qui seront appropriés pour des communications processeur-mémoire. L'utilisation combinée de WDM et de guides d'onde multiples conduit également à une bande passante globale élevée dans le réseau optique.

6. Conclusion et perspectives

Les interconnexions photoniques sur silicium sur puce ont le potentiel de surmonter les limites des interconnexions électriques traditionnelles en ce qui concerne les performances de communication, l'efficacité énergétique et le coût du matériel. Cependant, en raison des limitations technologiques actuelles, elle fait face à des défis car elle nécessite une intégration hétérogène de matériaux (par exemple, silicium, silice, Ge, etc.), de fonctions (processeur, mémoire, réseau de communication, etc.), et dedomaines (par exemple, électronique et photonique). Dans cette thèse, nous étudions l'amélioration de l'efficacité énergétique à partir de trois aspects: les topologies / layouts, la variation thermique et l'architecture.

**Topologies/layouts**

Du point de vue de la topologie et le layout physique, nous explorons plusieurs topologies et comparons leurs implémentations en utilisant des technologies monocouche et multicouches. Matrix, λ-router, Snake et ring ont été considérés. Le nombre de lasers, de MR, de photodétecteurs et de longueurs d'onde est estimé en fonction de la taille du réseau. Les résultats montrent que ORNoC dans la topologie en anneau évite l'utilisation des MRs dans les interconnexions optiques, conduisant à une perte optique plus faible. La limitation du nombre de longueurs d'onde peut être atténuée par l'ajout de guides d'ondes supplémentaires.

Les schémas physiques des topologies sont proposés et comparés. Pour Matrix, λ-router et Snake, deux nouveaux layouts sont proposés. Le premier type évite tout croisement de guide d'ondes (nommé layout^wX), et le second réduit la longueur de guide d'onde la plus défavorable entre les IP cœurs (nommée layout^X). Il est démontré que les implémentations de topologie
basées sur des anneaux présentent une plus grande efficacité énergétique par rapport aux implémentations de réseaux à base matricielle (c'est-à-dire topologie Matrix) et à plusieurs étages (c'est-à-dire, topologies λ-router et Snake).

Outre les implémentations de layout à couche unique, nous évaluons également les implémentations de layout multicouches correspondantes de différentes topologies en considérant la technologie de silicium déposée multicouche. Comme pour les implémentations de layout monocouche, deux layouts multicouches sont proposés pour les topologies Matrix, λ-router et Snake, dont un avec une longueur de guide d'onde minimisée (c'est-à-dire, layout\textsuperscript{wX}) et l'autre sans passage de guide d'onde (c'est-à-dire, layout\textsuperscript{w/oX}). Les résultats montrent que l'implémentation multicouche peut permettre une amélioration importante de la perte optique par rapport à l'implémentation monocouche. Pour un nombre différent de cœurs IP, la perte la plus faible et la perte moyenne sont réduites dans les implémentations multicouches. En particulier, cette réduction est plus grande pour les layouts qui présentent plus de croisements de guides d'ondes dans l'implémentation à couche unique.

**Variation thermique**

En raison de la distribution inégale de la consommation d'énergie sur la puce, le gradient de température peut exister dans des interconnexions photoniques en silicium. Cette variation a un impact négatif sur la fiabilité des communications et l'efficacité énergétique. Basé sur notre analyse de l'influence de la variation thermique, nous proposons une méthodologie pour concevoir une interconnexion photonique de silicium thermorésistant.

La méthodologie permet d'explorer l'espace de conception au niveau du périphérique et du système. A cet effet, les caractéristiques principales des dispositifs optiques (par exemple, les lasers, les MRs, les guides d'onde, les photodétecteurs) sont prises en compte dans les modèles au niveau du dispositif. Les aspects architecturaux tels que la taille des interconnexions et la topologie/layout sont pris en compte dans les modèles au niveau du système. A partir d'une activité de puce donnée, la simulation thermique permet d'estimer les profils de température dans la puce et les modèles analytiques permettent de calculer la consommation de puissance de calibrage et le BER. L'exploration de l'espace de conception peut ensuite être réalisée pour optimiser l'efficacité énergétique et la fiabilité des interconnexions optiques.
Nous proposons en outre une méthode de calibrage de laser à puce thermique pour surmonter la variation de longueur d'onde induite par la variation de température tout en réalisant en même temps un BER ciblé. Cette méthode dépend principalement du calibrage du courant du pilote laser. En conséquence, il syntonise à la fois la longueur d'onde du laser et les longueurs d'onde résonantes du MR le long d'un canal de communication, au lieu d'accorder seulement des longueurs d'onde résonantes du MR dans le procédé classique. De plus, afin d'estimer l'efficacité de la méthode proposée, nous avons mis en place un modèle de transmission et un modèle de puissance pour évaluer la fiabilité et l'efficacité énergétique respectivement dans le modèle de simulation que nous avons établi. Dans ces modèles, nous prenons également en compte la sensibilité thermique des sources laser sur puce. Les évaluations sont réalisées en prenant le schéma de communication MWSR comme une application illustrative de la méthode dans une architecture 3D empilée qui interconnecte plusieurs processeurs. En utilisant le simulateur thermique, nous pouvons obtenir des cartes de température détaillées sur toute la puce. Dans les simulations, nous utilisons différentes activités de puces pour explorer un meilleur compromis entre la fiabilité (par exemple BER) et l'efficacité énergétique. Grâce à cette exploration, nous proposons des stratégies pour minimiser la consommation d'énergie ou le BER. Nous explorons pour améliorer l'efficacité énergétique en utilisant un laser sur puce avec une efficacité plus élevé, réduisant ainsi l'impact de la variation thermique. A partir des résultats de la simulation, nous pouvons conclure que la méthode proposée qui combine le calibrage des lasers et des MRs présente des avantages significatifs sur la puissance de calibrage que la méthode conventionnelle qui n'ajuste les MRs que lorsque l'activité uniforme des puces diminue.

**CHAMELEON**

Pour utiliser les bonnes propriétés de l'exploration de topologies et layouts, nous proposons **CHAMELEON** basé sur la topologie en anneau, en utilisant à la fois des sens de communication dans le sens des aiguilles d'une montre (C) et anti-horaire (CC). Dans l'architecture CHAMELEON, les interfaces sont les composants du cœur, qui permettent de reconfigurer les canaux de communication comme MWSR, SWMR, MWMR et SWSR à la fois de conception ou d'exécution. Grâce à la reconfiguration des interfaces, différents schémas de communication peuvent être implémentés. Dans cette thèse, nous décrivons les schémas de configuration en temps de conception et de temps d'exécution: i) par application cartographique et ii) par protocole de communication. Pour la configuration en temps de conception, nous utilisons
l'application décodeur audio MP3 pour illustrer le processus de configuration. Pour le schéma de configuration d'exécution, nous proposons un protocole de communication et un algorithme d'allocation de ressources. Pour évaluer l'architecture proposée, nous utilisons le modèle de perte optique et la puissance de sortie laser minimale. Nous comparons l'architecture proposée avec trois architectures pour $2 \times 2$, $4 \times 4$ et $8 \times 8$ cœurs. Par rapport aux ONOCs passifs, CHAMELEON configuré pour mettre en œuvre la même connectivité conduit à 7,4% d'énergie. En outre, l'utilisation combinée des sens dans le sens des aiguilles d'une montre et dans le sens inverse des aiguilles d'une montre pour la propagation du signal dans CHAMELEON permet une amélioration substantielle de son efficacité énergétique et de son évolutivité.

Nous complétons la thèse avec les travaux futurs en trois aspects: i) le calibrage thermique du laser thermique au moment de l'exécution; ii) un modèle unifié de transmission MR; iii) voie de communication complémentaire pour réduire la puissance du laser.

7. Reference


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Chapter 1. General introduction

1.1. Communication trend and interconnect challenge

Nowadays, we live in an era of information explosion. Applications running on our computers and mobile devices, such as personal media, online business, medical monitoring, social media, and science education, are data intensive. Thus, it requires communication architectures with high performance and energy efficiency.

1.1.1. Datacenter and supercomputer

Datacenters and supercomputers are computational platforms for storage-intensive and computation-intensive applications respectively. They need to provide huge amounts of storage and computational resources to implement services. It was forecasted in a technical report from Cisco [1] that the annual global datacenter traffic will reach 8.6 zettabytes in 2018, among which a large percentage of the data transfer happens within the same datacenter. Thus, it requires high-speed data transfer between different processors and memories.

However, traditional copper cabling has become an obstacle for high-speed interconnects, due to its low data transmission speed, low bandwidth, and high power dissipation. For instance, in Tianhe-2 supercomputer (also called Milkyway-2 supercomputer), the cooling system (6.4MW) consumes around 30% of the total power (17.6MW for processors, memory and interconnect). The amount of the copper cabling has contributed most to this number since the cables block the cooling air flow.

Therefore, energy-efficient and environmentally friendly communication interconnects are of high interest. To reach an aggressive bandwidth goal, significant improvements on current interconnect technologies are needed.

1.1.2. Chip-to-chip

Computer architectures are increasingly utilizing multi-core processors and large volume memories [3]. Even though the performance of processors is enhancing due to increasing number of cores, the off-chip memory bandwidth is not likely to increase in a similar way. Future high-
performance multi-processor system will require bandwidths from 200 GB/s to 1.0 TB/s [2], to handle the communication between memories and processors.

Two main aspects limit the improvement of off-chip aggregated bandwidth: i) pin count is limited by the area and power cost of both high-speed transceivers and package interconnects; ii) signaling rate per pin is constrained by the overhead of energy efficiency, which will not be likely to increase dramatically without an innovative technology. This leads to a constraint on input/output (I/O) to access the main memory.

Thus, chip-to-chip communication interconnects become a bottleneck for the improvement of system performance. Currently, the mainstream chip-to-chip communication is based on electrical interconnects. Nevertheless, there is non-negligible distance to connect chip to chip, which results in a lower clock frequency. One way to alleviate this issue is to increase the count of parallel electrical wires and reduce the separation gap between wires. However, this could increase the coupling between neighboring wires, decreasing the supported clock frequency and in turn limiting to add more wires [58]. In addition, there are challenges in the aspects of channel loss, pin-count constraints, and crosstalk, resulting in the limitation of energy efficiency and bandwidth [59].

1.1.3. On-chip

Moore’s Law predicted that the transistor count on a given size of Integrated Circuit (IC) doubles every 18 months. As the transistor scales down, the performance improves in the meanwhile [4]. With size scaling of devices and increasing speed requirement, a power wall appears since the power density on a chip increases sharply with the speed to achieve. To keep things moving, the philosophy that a single core is divided into several cores with lower power consumption has inspired the era of multi-core [5]. Thus, multi-core processors appear as a solution to the traditional chip development, which improves the performance by increasing the number of cores. The requirement for a higher computing performance and the progressive technology scaling has pushed the trend to integrate more and more cores in a single chip.

However, the overall performance and energy efficiency cannot achieve a proper improvement due to the electrical interconnects [7]: capacitive and inductive coupling, parasitic resistance, interconnect noise, and big propagation delay of global interconnect. Especially, long wires are not advantageous for on-chip interconnects since they need repeaters every 1mm or
less to maintain signal quality [6]. Moreover, the requirement to improve power budget of inter-core communication is also increasing. For instance, about 80% of the total power budget is needed by the metallic interconnects at the technology node of 32nm [62]. Overall, given the increasing number of cores, challenges exist in the design of multi-core/many-core systems using traditional electrical interconnect [7].

1.2. **Emerging technology for interconnects**

Three major emerging technologies for interconnects are available: 3D stacking, radio frequency (RF), and silicon photonics.

1.2.1. **3D stacking**

International Technology Roadmap for Semiconductors (ITRS) previewed that the size of transistors will not shrink after 2021 (as shown in Figure 1). As reported, it will not be economical to locate more transistors onto a single chip by reducing their sizes. One possible alternative rationale for the chip manufactures would be to design multi-layers chips, thus shifting the focus from horizontal to vertical dimension.

![Figure 1: Roadmap of gate length. In the ITRS 2013 report, the physical gate length of transistors would reduce until 2018, while the ITRS 2015 report shows the length will stop shrinking after 2021 [8]. However, it is said that further scaling may be possible if the transistor geometry is turned from horizontal to vertical.](image)

3D stacking technology (e.g., silicon interposer, TSV-based manufacturing, monolithic 3D, etc.) enables multiple layers to be integrated in a same chip, and provides inter-layer interconnects. Compared with the traditional 2D chips, 3D stacking technology shortens the
global communication distance by using vertical interconnects, thus the latency and power can be reduced. It also reduces the footprint of the chip by using the vertical dimension.

This technology inspires the new vision in the development of semiconductor industry: how it will be designed, implemented, scaled, and used. More importantly, 3D-stacking technology offers a new design dimension [9], i.e., vertical. One promising enabling technology is to use Through-Silicon Vias (TSVs) [8]. It enables to stack multiple layers together by using TSVs. In this way, different layers with various characteristics (e.g., the electrical layer and optical layer, or the logic layer and memory layer) can be integrated together, which creates a new approach to scale. Thus, it provides the potential to overcome the limitation of scaling on the 2D surface of chip. This property in turn enables to improve the system performance, even as the scaling progress slows down (in Figure 1). Due to the property of stacking multiple layers, the technology also offers the possibility to optimize the various layers separately, which eases the whole design.

In industries, 3D stacking technology has been already used in some processor chips, but mostly they only stack memory with cores in different layers. IBM firstly announced the chip-stacking technology in a manufacturing environment in 2007 [10]. Heat dissipating is one of the main concerns for 3D stacking. Thus, the number of layers stacked in each 3D processor is not so many, 2-4 layers in general. In order to prevent thermal issues, in 2008 IBM demonstrated a prototype which integrates a water-cooled architecture in 3D stacking processor [11]. In 2011, IBM and 3M announced a new 3D stacking technology, which can stack 100 silicon chips together with silicon glue in the same package. They developed a new type of electronic glue, and it can interconnect different layers and conduct the heat away from the silicon package [12].

In academic, a lot of 3D interconnect architectures are proposed from the perspective of network, such as network topology [13], task mapping [14], routing algorithm [15][16]. There is also research about TSVs [17], circuit design [18], new architectures [19].

In addition, 3D stacking technology can be applied for memory, showing the improvement in aspects of performance [24][25] and energy consumption [26]. Recently, technology advancements in TSV-based 3D-stacked DRAM enables high-density application of TSVs, which eliminates the long global paths in 2D routing and allows new opportunities in data organizations to achieve low power and high bandwidth [28][29][30]. Based on the results in [27], the bottleneck related with DRAM scaling can be dealt with by strategically managing the
data in 3D-stacked DRAMs. Thus, the possible applications include “logic+memory” system-in-package (SIP) [21][22], heterogeneous multi-level Silicon-In-Package (SIP), 3D logic chip [23], high-density flash, image sensor, etc.

Overall, 3D stacking technology is an emerging solution to reduce the interconnect length. However, it also faces challenges in the aspects of cost, integration, thermal concerns [31] (related to increased power density because of the vertical stacking and reduced footprint), reliability, mismatch between various layers and yield induced by TSVs [32], which are interesting topics to study. Also, a solution to mitigate the impact is mandatory.

1.2.2. Radio frequency (RF)

Radio frequency (RF) refers to any of electromagnetic wave frequencies in the range from 3 kHz to as high as 300 GHz. Different RF signals have different frequencies. The electromagnetic wave is transmitted at the speed of light which equals to the product of the frequency and wavelength. Given that the light speed is fixed, the frequency is inversely proportional to the wavelength of the signal wave. The RF signals are generated by radio transmitters and received by radio receivers [37]. When the RF signal is propagating, it experiences the losses in the path, resulting in the attenuation of the RF signal.

RF signals can be transmitted in either free space or guided mediums [33]. For the transmission in free space, it has the similar form as an on-chip local area network, composed of transmitters, receivers, antennas, and necessary signal generation and detection circuitry. However, the efficient sending and receiving of RF signals require that the sizes of antennas should be comparable with their wavelengths [33]. For instance, for CMOS devices working at the frequency of 100GHz, the optimal aperture size of the antenna is of the order of 1mm², which is too large for the implementation of on-chip communication [33]. For the transmission in guided mediums, such as transmission line or waveguide, RF interconnect (named as RF-I for short) is possible to have low attenuation up to at least 200GHz [33]. However, RF-I also faces challenges [34] including: i) the crosstalk noise between adjacent transmission lines, especially at high frequencies or in long transmission lines; ii) area overhead and interconnect density; iii) limitation of drop points, leading to issue of scalability.
Figure 2: FDMA RF-I concept illustration, with 6 bands transmitting on the same physical transmission line [36].

Generally, RF-I is considered as a possibility to handle Gb/s data stream from chip to chip and on chip communications. Compared with traditional electrical interconnects, RF-I on chip (as shown in Figure 2 with 6 carriers) is demonstrated to have the advantages in terms of bandwidth, latency, energy efficiency, scalability, and re-configurability [37][38][39]. The primary advantages of RF-I are detailed as follows: i) the data are modulated onto electromagnetic carrier waves (at the speed of light) which will be continuously sent along the transmission line, instead of “1” and “0” represented by charging and discharging in the traditional electrical interconnect. Thus, it can save the propagation time and energy consumption. For instance, according to [38], the design which combines RF-I global links with local electrical interconnects is able to provide the inter-core network with either 1.7X performance gain under the same power or 5X power savings under the same performance; ii) the whole bandwidth is divided into multiple frequency domains, with each domain becoming a narrow-band signal channel which saves transmission power, and the bandwidth efficiency can be improved by sending many parallel streams of data over a single transmission line; iii) good scalability is achievable by adding more bands for the transmission in a similar way like in Figure 2, i.e., multiband RF-I, in order to obtain higher bandwidth utilization; iv) RF-I is capable to naturally support multicast of data with on-chip directional couplers [35], in the cost of higher provided signal power; v) reconfigurable of bandwidth allocation and location during compilation time or at runtime.
The feasibility of on-chip RF interconnects, the transmission property of on-chip RF-I, and the comparison with electrical interconnects are introduced in [36]. At the same time, RF-based Network-on-Chip (NoC) is proposed, named as MORFIC (Mesh Overlaid with RF InterConnect) [37]. The same group analyzed and discussed RFNoC from the point view of lower power design [38]. In 2009, the detailed introduction of a hybrid NoC which is based on wireless was carried out [40]. The possibility of integrating RF into 3D NoC was explored in [41]. Since 2011, RF-based NoCs have become one of the important research areas for on-chip communication [42] [43] [44][45][46].

1.2.3. **Silicon photonics**

Silicon photonics technology uses silicon as an optical medium. The maturity of silicon processing in the CMOS industry leads to the potentiality of low cost and large scale manufacturing capacity [47]. In addition, silicon can provide transparent transmission at the standard telecommunication wavelength, e.g., $\lambda=1550\text{nm}$. It is also feasible to integrate other materials to enhance the functionalities, such as silicon nitride, III-V compound semiconductors, group-IV elements and so on.

Silicon photonics has the potential to replace the traditional electrical interconnect for interconnects, just as fiber optics revolutionized the telecommunication industry by speeding up the transmission of information. Silicon photonic interconnects utilize optical carriers to transfer data from sources to destinations. It is a promising and revolutionary technology, which has advantages in aspects of transmission speed, aggregate bandwidth, and energy efficiency compared to the traditional electrical interconnects.

A significant advantage of silicon photonic interconnects is the ability to use wavelength division multiplexing (WDM), that is, to provide parallel wavelength channels by using different wavelengths of light. This property offers high bandwidth and performance. Moreover, by utilizing WDM, the bandwidth scalability is feasible by adding more available wavelengths in the propagation medium. Thus, instead of parallel physical optical links, WDM technology offers a cost-effective way to increase the bandwidth by using multiple wavelengths. In addition, silicon photonic interconnects are also advantageous in scalability, multicast communication, and re-configurability, just like RF-I.
As constituent parts, silicon photonic devices are available by employing the existing semiconductor fabrication techniques, which makes this type of interconnects more attractive to both academic research and industry (such as IBM, Intel, HP, and Cisco). Due to the compatibility with the conventional fabrication techniques, the optical and electrical functions can be integrated and fabricated into different layers of the same chip.

Benefited from the advanced property, the silicon photonic interconnects are promising for the communication architecture in a variety of applications, including on-chip systems, inter-chip systems, and data center/supercomputer.

1.2.3.1. Datacenter

Silicon photonics is a promising option for interconnects within datacenters [48][49], by using optical fiber as data transmission medium. It has the potential to address the increasing bandwidth requirement of datacenters [50][51][52], including video, voice, data and cloud service. Moreover, it can improve energy efficiency in datacenter. For instance, by using optical fibers for connection, it can make the rack equipment “slimmer”, leading to lower power consumption in cooling.

![Figure 3: illustration of co-packaged WDM transmitter with N×28 Gb/s data paths [53].](image)

A four-channel implementation of a WDM-based silicon photonic transmitter (data rate of 4×28 Gb/s) and modulator array (date rate of 4×32Gb/s) are demonstrated respectively in [53] and [54] in 2015. By using integrated lasers, the photonic transmitter is scalable to higher channel count for WDM-based communication, as shown in Figure 3.

In 2015, IBM announced the first fully integrated wavelength multiplexed silicon photonics chip, enabling the manufacture of 100 Gb/s optical transceivers and allowing both the optical and electrical components to exist side-by-side on the same package. This can be seen as a significant milestone in the development roadmap of silicon photonics technology, which will allow
datacenters to offer greater data rates and bandwidth capacity for cloud computing and big data applications in the future.

Figure 4: Several hundred chips intended for 100 Gb/s transceiver, diced from wafers fabricated with IBM CMOS integrated Nano-Photonics technology. The dense monolithic integration of optical and electrical circuits and the scalable manufacturing process provide a cost-effective silicon photonics interconnect solution, suitable for the deployment in cloud servers, datacenters, and supercomputers (Source from IBM).

1.2.3.2. Chip-to-chip

Silicon photonics can also be used to relieve the communication bottleneck between different chips on the same board [55], since chip-to-chip I/O speed will be limited by the conventional electrical interconnects. High-speed I/O technology using silicon photonics offers high-performance interconnects for chip-to-chip communication and energy-efficient scaling of data rate, by adopting WDM.

In industry implementation, Intel has made significant progress to demonstrate the feasibility of optical chip-to-chip interconnects [56]. In 2010, Intel demonstrated a system using silicon photonics to transmit data between printed circuit boards at 50 Gb/s. The prototype was done with a hybrid silicon/indium phosphide laser, a silicon modulator operating at 40 Gb/s, a germanium photodetector, and a four-channel photonic link with each channel operating at 12.5 Gb/s.

In academic research, a chip-to-chip silicon-photonic link with optical devices and electronic devices integrated on a same chip is demonstrated in [57], as shown Figure 5. Optical signals with different carrier wavelengths are introduced into the silicon interconnect to form various wavelength channels.
Figure 5: A chip-to-chip DWDM optical link using silicon-photonics [57].

From the work presented in [57], a 2.5 Gb/s optical link between a dual core processor and 1MB memory on separate chips is demonstrated by researchers from the University of California, MIT, Berkeley, and the University of Colorado Boulder [59]. This is a realization of a microprocessor which uses on-chip photonic devices to directly communicate with other chips using light. All the components are fabricated based on standard CMOS process, without change at the manufacturing process. Three external optical interfaces are used: one for coupling the light from off-chip laser to the chips, another for data from processor to the memory, and the last one for the data from memory to the processor. It reaches an aggregate bandwidth of 5Gb/s.

1.2.3.3. On-chip

Silicon photonic interconnects on chip (shown in Figure 6) is a prospective choice for the communication architecture of future high-performance many-core processors, alleviating the bottleneck of global electrical interconnects. It is elevated by the recent advances in silicon photonic devices and 3D stacking technology. The transmission delay and power consumption in photonic interconnects are almost independent of the distance. For instance, optical signal transmits at much higher speed (i.e., $66600\text{km/s} \rightarrow 15\text{ps/mm}$ [61]) without intermediate store-and-forward, providing lower end-to-end delay compared with using electrical interconnects. High bandwidth can be achieved by using WDM technology. For example, each wavelength can provide a bandwidth of more than 10 Gb/s and up to 64 wavelengths [60] can be used in each optical interconnect at the same time.
Both academic research [20][64][65] and industry [66][67] are making efforts to design high-performance on-chip silicon photonic interconnects so as to meet continuously increasing requirement of inter-core communication. In industries, IBM announced a 1Tbps parallel interconnect using external vertical-cavity surface-emitting lasers (VCSELs) and photodetectors in 2012 [66]. STMicroelectronics grants Luxtera’s silicon photonics technology on low-cost high-volume components and systems being implemented in ST’s new photonics process at its wafer lab in France [67].

1.3. Challenges and thesis outline

Silicon photonic interconnects have several prospective advantages such as low transmission latency, high bandwidth, and high energy efficiency. However, due to technology limitations, it still encounters challenges [68][69] in manufacturing issues, opto-electrical integration, reliability, energy efficiency, photonic design automation, etc. In this thesis, we focus on design methodologies for energy-efficient silicon photonic interconnects on chip related to topology/layout, thermal variation, and architecture.
- **Topology/layout**: Different topologies and physical layouts provide various interconnection options for on-chip communication. This leads to a large variation in optical losses. An optimized topology or layout would reduce the power consumption of the laser source. Thus, design space exploration is needed to improve the energy efficiency.

- **Thermal variation**: Due to the uneven distribution of power consumption over the chip and the thermal sensitivity of photonic devices, thermal variation exists in on-chip silicon photonic interconnects. This significantly impacts communication reliability and also energy efficiency. In order to mitigate the influence of thermal variation, a solution is required which is able to improve the energy efficiency and maintain the communication reliability in the meanwhile.

- **Architecture**: The communication schemes and resource assignments lead to different routing paths between sources and destinations, which contributes differently to overall energy efficiency. Therefore, an architecture with an optimized communication scheme is needed.

The rest of this thesis is organized as follows:

Chapter 2 gives an overview on the state of art of silicon photonic interconnects on chip. We first introduce on-chip silicon photonic interconnects technologies. Then the optical devices are reviewed. Proposed architectures are outlined, and two variations (i.e., process variation and thermal variation) related research are presented. The modeling and simulation platforms are summarized. Finally, the main challenges to address in this thesis are highlighted.

Chapter 3 explores on-chip silicon photonic interconnects with various topologies and physical layouts to provides design guidelines. This chapter studies popular topologies, including Matrix, λ-router, Snake, and ring crossbars. Then, physical layouts for both single-layer and multi-layer implementations are proposed. We also establish a loss model to evaluate the worst-case optical loss.

Chapter 4 proposes a thermal-aware design methodology in order to improve the energy efficiency while meet the requirement of communication reliability. This chapter begins with the analysis on the influence of thermal variation in silicon photonic interconnects on chip. Then, the proposed thermal-aware design methodology is presented. The transmission model, power model,
and simulation model are given, which allows reliability and energy efficiency of optical interconnects to be evaluated.

Chapter 5 proposes a channel efficient optical network on chip, named CHAMELEON. This architecture can improve energy efficiency and utilization of optical interconnects by flexibly configuring the optical interconnection between sources and destinations. In this chapter, the network architecture is introduced at first. Then, the configuration methods are presented, including application mappings at design time and communication protocol at run time. Finally, the energy efficiency of the proposed architecture is evaluated.

Chapter 6 concludes the thesis and discusses the perspective work in the area of silicon photonic interconnects.

1.4. References


Chapter 1 General introduction


Chapter 1 General introduction


Chapter 2. State of art of silicon photonic interconnects on chip

With the fast development of chip-scale optical devices, silicon photonic interconnects become promising for on-chip communication. In this chapter, we first give an overview on silicon photonic interconnects in Section 2.1. In Section 2.2, optical devices are introduced, as well as an emerging technology (i.e., multi-layer deposited silicon technology) to implement the optical devices. In Section 2.3, photonic networks are presented and two types of variations are described. In Section 2.4, system-level and device-level modeling and simulation approaches are introduced. Finally, in Section 2.5, energy efficiency challenges to address in this thesis are introduced.

2.1. Overview

Silicon photonic interconnects on chip have the potential to provide superior properties of low latency, high bandwidth and low power consumption [1], compared to traditional electrical interconnects. As shown in Figure 7, they are basically composed of optical devices such as laser sources, waveguides, Microring Resonators (MRs), and photodetectors.

![General view of silicon photonic interconnects on chip in indirect modulation method](image)

Figure 7: General view of silicon photonic interconnects on chip in indirect modulation method [2].

Laser sources are used to emit optical carriers. The electrical signals are modulated onto optical carriers in either direct (i.e., modulating at the laser sources) or indirect (i.e., modulating at the modulators) method. For instance, each data bit “1” or “0” can be represented by the presence or absence of the carrier in on-off keying (OOK) modulation. After modulation, optical signals transmit in waveguides from the source to the destination. At destination side, optical
filters drop the optical signals into photodetectors and then the photodetectors convert the optical signals back into electrical domain.

2.2. **Introduction of optical devices**

Silicon photonic interconnects are implemented with optical devices in an optical layer [49]. The main optical devices are introduced in the following subsections.

2.2.1. **On-chip lasers**

Laser sources provide optical power for communication in silicon photonic interconnects on chip. According to their locations, the laser sources can be categorized into two types: off-chip and on-chip. Off-chip lasers need couplers and power waveguides to distribute the optical power into the silicon photonic interconnects. On-chip lasers and photonic interconnects are integrated in the same chip, without the need to couple the optical power onto the chip. Thus, on-chip lasers avoid the loss from the coupler and power waveguides.

Compared with off-chip lasers, on-chip lasers have the potential to provide the following three key advantages:

- **Lower integration complexity and more efficient integration by relaxing the physical constraints on layout:** in case of on-chip lasers, it is not necessary to distribute the light from an external source to the modulators (e.g., through the so-called *power waveguide* [52]). Relaxing such constraints contributes to reducing the number of waveguide crossings or even avoiding them altogether in the ring topology.

- **Higher scalability by keeping the lasers fully distributed over a chip,** which is not achievable by considering centralized off-chip lasers.

- **Lower power consumption by reducing the worst-case communication distance,** which corresponds to the distance from the source IP (intellectual property) core to the destination IP core for on-chip laser based architectures. However, for off-chip laser based architectures, it additionally includes the distance from the off-chip laser to the source IP core. Shorter distance, consequently, reduces the optical losses and hence the minimum required laser output power. Moreover, the power consumption can be further improved by locally turning off the on-chip laser when no communication is required.
As for the WDM technology in the communication, laser arrays (i.e., one laser for one wavelength) or one multi-wavelength comb laser (e.g., a quantum dot comb laser) are possible options to realize the multiple wavelength emission [3].

Laser sources can be fabricated in several ways and rely, for instance, on Microdisk, Fabry-Perot (FP), distributed feed-back (DFB) and distributed Bragg reflector (DBR) [4]. Among the available technologies, vertical-cavity surface-emitting lasers (VCSELs) provide an optical output power in the range of hundreds of microwatts, thus meeting the requirements for nanophotonic interconnects [4]. Furthermore, VCSELs based on a double set of Si/SiO$_2$ photonic crystal mirrors (PCMs), so called PCM-VCSELs (as shown in Figure 8), are CMOS-compatible [5][6]. They can be used as on-chip laser sources since their footprint is of the same order of magnitude as the size of a MR used to modulate continuous waves emitted by off-chip lasers. VCSELs are thus sufficiently compact to be implemented in a large number. In this way, it saves the laser power since losses caused by power waveguides [52] are avoided, compared with off-chip lasers. Thus, PCM-VCSELs [5][6] are assumed in our work for on-chip lasers. Indeed, CMOS-compatible VCSELs allow direct modulation or indirect modulation of the optical signals.

![3D view of PCM-VCSEL](image)

Figure 8: 3D view of PCM-VCSEL [7].

2.2.2. Waveguides

Waveguides are the transmission medium to carry the optical signal over the chip. In silicon-on-insulator (SOI) technology, it generally uses silicon as core (refractive index is about 3.5) and silica as cladding (refractive index is about 1.5) [8]. Due to the high refractive index contrast between silicon and silica, the waveguide keeps a tight confinement of the light for transmission [8]. Also, because of the high refractive index of silicon, it allows submicron-scale waveguides with small bending radii [9]. This kind of waveguides can be fabricated easily in silicon-on-insulator (SOI) processes which are widely available for CMOS. The cross-section dimension of
a waveguide is usually in the order of hundreds nanometers, e.g., 460nm×200nm (Width × Height) [10][11].

![Cross-sectional structure of a typical silicon photonic waveguide](image)

**Figure 9: Cross-sectional structure of a typical silicon photonic waveguide [10].**

Nevertheless, when the optical signal is propagating in the waveguides, optical losses may occur, such as propagation loss (due to scattering and absorption at the sidewalls), bending loss, etc. One way to reduce the loss is to utilize other materials, for instance, silicon nitride, which is reported to induce lower propagation loss than crystalline silicon [38]. In addition, when two waveguides cross each other and have an intersection, crossing loss occurs which is also a main source of optical losses. To mitigate this kind of loss, a proper topology or multiple-layer implementation can be of help.

### 2.2.3. Microring Resonators (MRs)

The Microring Resonator (MR) is a critical photonic component for silicon photonic interconnects on chip. A generic MR consists of a waveguide which forms a loop in itself [11], usually placed adjacent to another waveguide. MRs can be fabricated based on PIN junction or PN junction. Compared to PN-based MRs, PIN-based MRs are preferred due to high extinction ratio, low optical insertion loss, and low driving voltage required, which contributes to higher energy efficiency. The disadvantages, i.e., low date rate, can be alleviated by using WDM [3].

A MR only becomes useful when there is a coupling to the outside world [11]. The coupling, known as a resonance, occurs when the optical path length of the MR is exactly a whole number of wavelengths. Thus, the primary optical characteristic of a MR is its resonant wavelength.
When the wavelength of a signal in the waveguide is as same as the resonant wavelength of MR (as illustrated in Figure 10-a), the signal is coupled into the MR; otherwise, it passes by the MR unaffected (as illustrated in Figure 10-b).

![Figure 10: MR operation: a) signal wavelength ($\lambda_{signal}$) equals to MR resonant wavelength ($\lambda_{MR}$), and b) signal wavelength ($\lambda_{signal}$) is different from MR resonant wavelength ($\lambda'_{MR}$).](image)

The resonant wavelength of the MR is determined by the device geometry and the refractive index. It can be controlled by applying microelectromechanical [12], optical [13], electro-optic [14][17] and thermo-optic [18] mechanisms. The last two types of mechanisms draw more attention in the current research, introduced as following:

**i) Voltage Tuning (VT):** Due to the electro-optic effect, the resonant wavelength of MR can shift. For instance, MRs based on forward-biased PIN junctions and reverse-biased PN junctions can change the resonant wavelengths by carrier injection and carrier depletion, respectively. Voltage tuning is fast but its range ($VTr$) is limited to 1nm [60]. We denote $VTe$ as the voltage tuning efficiency (typically 0.13mW/nm [19][65]).

**ii) Thermal Tuning (TT):** The MR resonant wavelength can be shifted by means of the local micro-heater [20]. Due to the thermo-optic effect of silicon-based optical devices, the resonant wavelength will shift towards right, when the temperature increases. Thermal tuning is slower than voltage tuning but its operating range ($TTr$) can reach 20 nm [21]. The thermal tuning efficiency $TTe$ is lower (typically 0.24mW/nm [19][65]).

Due to the property of wavelength selective, MRs can be used for modulators [14] (e.g., Figure 11), filters [15], and switching elements [50]. MR-based modulator can reach as large as 50Gb/s [16].
Figure 11: a) Schematic layout of the MR-based modulator; b) DC measurement of the MR, with the transmission spectra of the MR at different bias voltages (e.g., 0.58V, 0.87V and 0.94V, respectively). The inset shows the transfer function of the modulator for light with a wavelength of 1573.9nm [14]. (The figures are extracted from ref. [14])

2.2.4. Photodetectors

Photodetectors are used to convert the optical signal back into electrical signal. They can use III-V compound [23], implanted silicon [24], and germanium (i.e., Ge) [25][26][27]. To grow germanium on silicon has been widely researched for high-speed photo-detection on silicon photonic chips (as illustrated in Figure 12), due to its high absorption coefficient at the wavelengths of both 1.31um and 1.55um [26]. The low bias voltage of Ge-on-silicon photodetectors makes them a promising choice for integration with CMOS drivers [28]. For WDM application, the photodetector can be integrated with individual MRs to filter and then detect the optical signals at different wavelengths, as demonstrated in [25]. An important metric to measure the performance of a photodetector is responsivity (in A/W) [22]. It is defined as the converted photocurrent divided by the optical power at the input port of the photodetector.

Figure 12: An integrated Ge photodetector on a silicon waveguide [26].
In order to fully process the converted electrical signal, the photodetector need to connect with transimpedance amplifier (TIA), comparator and data recovery to form a receiver [29]. For a reliable and energy-efficient communication, two parameters are important: BER and receiver sensitivity (in dBm). BER is defined as the ratio of the number of the incorrect received bits to the number of received bits over a given time period. Receiver sensitivity indicates the minimum received optical signal power to reach a given BER.

2.2.5. Emerging multi-layer technology of optical devices

Emerging design technology based on multi-layer deposited silicon enables the efficient stacking of optical layers [30][31][38][39]. Multi-layer deposited silicon contributes to reduce the number of waveguide crossings, but leads to new optical losses related to inter-layer coupling. Thus, a design trade-off needs to be explored, in order to improve the interconnect energy efficiency.

2.2.5.1. Multi-layer deposited silicon technology

![Waveguide crossing in single-layer](image)

![3D view of waveguide crossing in different layers](image)

![Optical Vertical Coupler (OVC) based on](image)

Figure 13: a) waveguide crossing in single-layer [38], b) 3D view of waveguide crossing in different layers [38], and Optical Vertical Coupler (OVC) based on: c) inverse tapers [32] and d) MMI [33].

With multi-layer deposited silicon technology, waveguide crossings can be avoided, as illustrated in Figure 13-a and Figure 13-b. The multi-layer implementations rely on Optical
Vertical Couplers (OVCs) implemented by using inverse tapers (in Figure 13-c) [32], multimode interferences (MMIs) (in Figure 13-d) [33], MRs [34][35] or grating-assisted vertical couplers [36][37]. The coupling efficiency between the two waveguides, e.g., inverse tapers based, depends on the physical dimensions of the waveguides (i.e., height and width), the properties of the taper (e.g., type of material) and their location on the circuit (i.e., vertical gap, tips longitudinal overlapping and taper angle) [32].

The propagation losses can also be reduced by considering, for instance, silicon nitride ($\text{Si}_3\text{N}_4$) deposited on top of a standard silicon on insulator (SOI) [40][41]. In other words, once an optical signal reaches the top layer, it will experience lower propagation losses compared to signal propagating in bottom layer. However, reaching the top layer is possible only by crossing OVCs, which leads to additional losses (e.g., 0.2dB and 0.1dB reported in [40] and [38], respectively).

### 2.2.5.2. Multi-layer photonic interconnects

Multi-layer technology allows the reduction in number of waveguide crossings, reducing waveguide crossing losses (typically from 0.05dB [38] to 0.2dB [48] per crossing) existing in single-layer implementations. It decreases the total loss of the whole optical path, but it also introduces new losses due to the vertical coupler (typically around 0.1dB [33]). Therefore, multi-layer technology is highly suitable for optical architectures characterized by a high number of crossings. In this context, the works of [42], [43] and [44] present four-layer ONoCs using Multiple-Write-Single-Read (MWSR) communication scheme. The authors of [42] present a static optical crossbar, named MPNOC. In [43] and [44], the authors present reconfigurable architectures based on [42]. It employs MRs located on different layers to allow the re-allocation of the optical bandwidth between optical layers.

### 2.3. Silicon photonic interconnects on chip

In this section, two general types of silicon photonic interconnects on chip are first discussed. Then, two variation problems and related works are introduced and summarized.
2.3.1. **General types of photonic interconnects**

Currently proposed silicon photonic interconnects can be divided into two classes: optical crossbars-based and optical circuit switching-based. Compared to optical circuit switching-based interconnects, optical crossbars-based interconnects do not need preliminary path setup process.

2.3.1.1. **Optical crossbars-based interconnects**

In optical crossbars-based interconnects, the communication between a source IP core and a destination IP core is carried out through one wavelength or a set of wavelengths by using WDM. The popular optical crossbars are: Single Writer Single Reader (SWSR), Multiple Writers Single Reader (MWSR), Single Writer Multiple Readers (SWMR), and Multiple Writers Multiple Readers (MWMR). Table 1 summarizes the main characteristics of SWSR, MWSR, SWMR and MWMR.

<table>
<thead>
<tr>
<th>Approach</th>
<th>Latency</th>
<th>Power efficiency</th>
<th>Reusability</th>
<th>Resources</th>
</tr>
</thead>
<tbody>
<tr>
<td>SWSR</td>
<td>xxx</td>
<td>xxx</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>MWSR</td>
<td>x</td>
<td>xx</td>
<td>xxx</td>
<td>xx</td>
</tr>
<tr>
<td>SWMR</td>
<td>xxx</td>
<td>x</td>
<td>xxx</td>
<td>xx</td>
</tr>
<tr>
<td>MWMR</td>
<td>x</td>
<td>x</td>
<td>xxx</td>
<td>xxx</td>
</tr>
</tbody>
</table>

2.3.1.1.1. SWSR

SWSR statically assigns a specific wavelength for each pair of source and destination, creating dedicated point-to-point communication channels between IP cores. That is to say, the signals between different pairs of sources and destinations are routed according to their wavelengths. Thus, it has the advantage of low latency, due to the fact that the communications between IP cores are not influenced by each other (i.e., communication parallelism). For instance, \( \lambda \)-router, based on passive MRs and wavelength routing, is proposed in [51] (in Figure 14-a). Different pairs of sources and destinations are identified with different wavelengths. Thus, a truth table for wavelength assignment is needed, as illustrated in Figure 14-b. Another example of is Snake [46]. It is also a wavelength routed optical network providing point-to-point connections between IP cores.
Moreover, SWSR allows wavelengths to be reused in a same waveguide to design energy-efficient point-to-point channels. It implies concurrent communications in the whole interconnects, i.e., non-blocking network. For instance, ORNoC [47] (in Figure 15) is based on SWSR approach. The same wavelength (e.g., in red color) is used for non-overlapping communications in the same waveguide. It does not induce any waveguide crossings thanks to the ring topology and the use of on-chip laser sources, which leads to more energy-efficient data transmission. The main disadvantage of the SWSR approach is the lack of scalability. The scalability is limited by the number of the available optical sources (e.g., the number of wavelengths in one waveguide, available laser wavelengths, etc.). This scalability issue can be partially leveraged by using reduction method [45], but it comes at the price of limited connectivity which in turn impacts the reusability feature.

2.3.1.1.2. MWSR

MWSR assigns multiple wavelengths and a specific wavelength to each IP core for writing and reading signals, respectively. For a given IP core, there is an optical channel. Each source needs to request an access to the optical channel to communicate with a given destination. This
requires an arbitration to avoid writing conflict among writers, which can lead to extra latency, i.e., lower performance. Compared to MWMR, it improves the latency at the destination side but reduces the resource utilization. For example, Corona [52] utilizes an optical, token-based arbitration scheme to solve the conflict among writers. The source modulates the data at the same wavelength as the destination (in Figure 16).

![Figure 16: A four wavelength data channel example in Corona [52].](image)

### 2.3.1.1.3. SWMR

SWMR assigns to each IP core one specific wavelength and multiple wavelengths for writing and reading signals, respectively. It is able to implement a permanent broadcast among all IP cores. For instance, in ATAC [53], the optical network is used for global broadcasting. Even though no arbitration is needed, it is not an energy-efficient solution for point-to-point communication since the signal is transmitted from the source to all the other IP cores besides the destination. To overcome this limitation of energy efficiency, reservation scheme can be employed before sending data. For example, in Firefly [54] (in Figure 17), the power hungry broadcasting for the data is avoided by implementing reservation channels.
2.3.1.1.4. MWMR

MWMR allows all the writers and readers accessing the communication interconnect by using the arbitration strategy and dynamically assigning wavelengths for communication. In this way, the resource utilization (i.e., the wavelengths) is improved. However, to assign the wavelengths, there is a need of arbitration, leading to an overhead of latency. For example, FlexiShare [2] (in Figure 18) uses a token-stream based arbitration scheme to solve the contention at the writers’ side. At the readers’ side, a reservation assisted scheme is used to activate the corresponding destination through reservation channels. Then, the source sends the data at one wavelength to the destination.

2.3.1.2. Optical circuit switching-based interconnects

Optical circuit switching-based interconnects are composed of an optical data network based on circuit-switching and an electrical control network based on packet-switching. The
transmission of an optical message needs two steps. First, the electrical path-setup packets are routed in the electrical control network. During its propagation, the electrical packet reserves the optical resources (i.e., MRs) along the path to the destination, in order to set up an optical path for the optical message. Second, after successful setting up path, the optical message is transmitted directly from the source to the destination, without relaying or buffering. For instance, Figure 19-a shows an example of the basic optical router and Figure 19-b illustrates the process of path setup.

Many networks are proposed based on various topologies, such as crossbar [49], non-blocking Mesh [49][50], torus [55], 2D folded torus [56][57], fat-tree [58]. However, the potential advantage of optical interconnects is limited by the path-setup process. Therefore, the ratio of the optical path lifespan versus setup overhead can be a metric of the efficiency.

![Basic optical router](image1)

![Qualitative timing diagram](image2)

Figure 19: a) Basic optical router based on MRs, b) qualitative timing diagram of a successful optical path setup and a blocked setup request (extracted from [56]).

### 2.3.2. Process and thermal variations in silicon photonic interconnects

Optical interconnects encounter reliability issues due to process variation and thermal variation. They lead to drifts of the resonant wavelengths in optical devices. The mismatch between the actual resonant wavelength and the designed one decreases received signal power and increases crosstalk noise, which in turn increases Bit Error Ratio (BER). This reduces the energy efficiency and may lead to signal re-transmission.

#### 2.3.2.1. Process variation

Process variation refers to the fabrication-induced variations of the geometry of silicon photonic devices (e.g., waveguide width and height) during the manufacturing process, leading to the variation of the optical response of optical devices (e.g., the drift of MR resonant wavelength) [59][60][61][62][63]. For instance, the resonant wavelength of MR changes largely...
with the width variation: 1nm width variation induces approximately 0.583nm resonant wavelength drift [60].

To model the process variation, VARIUS [64] can be adopted or adapted since the characteristics of the variations in optical devices are close to that in CMOS devices [65][79]. Analytical models [66] and numerical techniques [67][68] are developed based on existing approaches to study the process variation in silicon photonic devices.

In the fabrication process, the uniformity can be improved by using corrective etching [69] or adaptive process control through exposure dose optimization during the optical lithography process [70].

After the fabrication, to solve the challenge of process variation, device-level and system-level solutions have been proposed. At device level, the process variation can be compensated by using thermal tuning [60][71][72], voltage tuning [60][71], and bandwidth tuning [73].

At system level, tuning MRs resonant wavelengths and re-assigning wavelength channels are proposed to compensate the process variation, while minimize the tuning power at the same time [75][76][77]. The similar idea of tuning can be used together with spare MRs [65]. Encoding schemes are proposed to mitigate the crosstalk noise induced by process variation [78][79]. Moreover, in [60], it is proposed to compensate chip-scale process variation by thermal management.

2.3.2.2. Thermal variation

Thermal variation refers to spatial and transient temperature fluctuation of optical devices due to the power consumption over the chip. This leads to variations of optical response of optical devices due to the thermo-optic effect of the material [60]. For example, the thermal variation of MR resonant wavelength can reach 0.11nm/°C [60].

At device level, solutions relying on athermal devices [74][80], voltage tuning [81], local heating [82][103], thermal-aware MR synthesis [83], and feed-back control schemes [84] have been explored to control or limit the thermal impact on the resonant wavelengths of MRs.

At system level, the analyses allow the influence of temperature variation on the optical signal power received by receivers to be evaluated [85][86]. Channel hopping, along with additional MRs on the ends of the spectral range, is utilized for tuning in [19][86][91][92]. For
instance, in [86], the thermal tuning is adopted to adjust the MR resonant wavelength to the neighboring channel wavelength.

Dynamic Voltage Frequency Scaling (DVFS), workload migration techniques, and job allocation policy can be applied to reduce the temperature variation [60][87][88][89]. For instance, in [88], a thread migration is adapted in cooperation with a temperature prediction model, in order to maintain the temperature of each core below a specified thermal threshold. By taking into account the thermal variation, the placement and sharing scheme of lasers have also been explored to reduce power consumption. In [90], the authors explore the placement of shared on-chip lasers (in Figure 20), which are located on a layer on top of the optical interconnects.

![Flowchart for deciding the sharing and placement configurations of on-chip laser sources](extracted from [90]).

In [93], the laser output power is reduced until BER requirements can still be reached for optical interconnects using on-chip lasers (with the tuning flow shown in Figure 21). The MRs wavelength mismatch is first compensated with electrical tuning; then (i.e., once the wavelengths are aligned), the laser output power is reduced. However, the impact of the driver current on the laser temperature is not taken into account, which will significantly impact: i) the laser output power and ii) the emitted signal wavelength. Moreover, the optical crosstalk for the signal is not taken into consideration, which may significantly impact the BER.
After the occurrence of bit error, code correction solution can be applied to mitigate the reliability problems. For instance, in [94], the authors propose using error detection codes and forward error correction codes to detect and correct various types of errors, respectively.

2.4. Modeling and simulation

To design and evaluate the silicon photonic interconnects on chip, modeling and simulation is necessary to model the functionality and evaluate the performance. The abstraction can be principally found in two levels: system level and device level. The device level refers to the basic devices, while the system level refers to topology/layout and architecture. The two levels can be coupled with each other to fully explore the design space. For instance, the performance, power and thermal simulators can be integrated and coupled together [123], as shown in Figure 22. Sniper [99] is used for performance simulation and is interfaced with McPAT [115] for power consumption evaluation of the system. Then, the power traces generated by McPAT are input to a 3D extension version of HotSpot [119] for thermal simulation. In the following subsections, we discuss the related work in these two levels.
2.4.1. System level

System-level simulations allow functional validation and performance estimation. For chip-scale interconnect network, there are generally two types: cycle-based and event-driven.

Cycle-based simulation drives networks cycle-by-cycle, thus leading to detailed cycle-accurate simulation. It is accurate, but slow. The simulators are typically single-threaded, which limits the simulation performance in multi-core era [99]. Moreover, the slow simulation speed is a constraint in simulating huge dynamic instruction counts in a given period of time [99]. Cycle-based simulators such as OMNeT++[95] and Booksim [101] are proposed in research to obtain more accurate results.

Event-driven simulation proceeds by checking an event queue. It is another simulation method at a higher abstraction level for simulating multi-core/multiprocessor systems [99], such as POINTS [56], Sniper [99], JADE [104], PhoenixSim [102], Gem5 [100], and Graphite [98]. The simulators can be realized, for instance, by SystemC [96] or C++. For instance, an ONoC is modeled in SystemC [97] at a high abstraction level, with the performance values extracted from physical level with specific tools and models.

DSENT (Design Space Exploration of Networks Tool) [103] is a unified framework for photonics and electronics (shown in Figure 23). It enables rapid area/power evaluation of opto-electronic on-chip interconnects. In addition, DSENT can be used to generate traffic-dependent power traces and area estimations for a network when integrated with an architecture simulator.
Event-driven simulation can achieve cycle-accurate simulation if it triggers the events by every cycle, at the cost of scheduling events. When there are few events, event-driven simulation performances well. Otherwise, it is almost the same with the cycle-based simulation.

In addition, placing and routing of ONoCs have been investigated [105][106]. For instance, PROTON [105] is a CAD tool to automatically place and route the optical elements from topology logic schemes to their physical implementation. The main properties of several placement and routing tools are shown in Table 2.

Table 2: Comparison of placement and routing tools for ONoCs (extracted from presentation of [106]).

<table>
<thead>
<tr>
<th>Tool</th>
<th>Placement</th>
<th>Routing</th>
<th>3D</th>
<th>Minimize Laser Power Consumption</th>
<th>Speed of Placement</th>
</tr>
</thead>
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<tr>
<td>Seo+ ISQED’05 [107]</td>
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<td>✓</td>
<td>x</td>
<td>x</td>
<td>N/A</td>
</tr>
<tr>
<td>Minz+ TCPT’07 [108]</td>
<td>x</td>
<td>✓</td>
<td>✓</td>
<td>x</td>
<td>N/A</td>
</tr>
<tr>
<td>Ding+ DAC’09 [109]</td>
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<td>✓</td>
<td>✓</td>
<td>N/A</td>
</tr>
<tr>
<td>Condrat+ TCAD’14 [110]</td>
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<td>✓</td>
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<tr>
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<tr>
<td>PROTON+ ICCAD’13 [105]</td>
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<td>–</td>
</tr>
<tr>
<td>PLATON+ ISPD’16 [106]</td>
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<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>+</td>
</tr>
</tbody>
</table>

2.4.2. Device level

At device level, power dissipation is related with the thermal variation, which influences the reliability in the architecture. Thus, power analysis and thermal tools are crucial in simulation. Wattch [113] is a widely-used processor power estimation tool to generate the power traces of the system. Orion [114] is a tool for modeling power in NoCs. McPAT [115] is an integrated
power, area and timing modeling framework for multithreaded and multicore/manycore processors. For thermal analysis, simulators such as ISAC [116], Hot-Spot [119], and IcTherm [117] are used to generate the temperature profiles of the system.

Therefore, for the modeling of the optical circuits, there are several choices including: i) Programming language, e.g., Matlab [120], C++, Verilog-A; ii) Open-source solutions, e.g., Orion [114]; iii) Commercial tools, e.g., MODE [118] for process variation analysis, Lumerical INTERCONNECT [121], EDA toolsets [122].

2.5. Design challenges in energy efficiency

In spite of the prospective advantages such as high bandwidth, low latency and distance-independent power dissipation, silicon photonic interconnects still have energy efficiency challenges due to optical losses, process variation, thermal variation, crosstalk noise. The following subsections introduce three identified main challenges we address in this thesis.

- **Topology/layout**

  Chip-level optical communication in silicon waveguides incurs more losses than fiber-optic communication (dB/cm vs. dB/km). Careful optimization of optical paths from the light sources is needed to achieve high energy efficiency. Thus, network topologies and layouts need to be explored.

- **Thermal robustness**

  The thermal variation increases BER and decreases energy efficiency of silicon photonic interconnects on chip. This is further accentuated by the significant reduction of on-chip laser efficiency as the temperature increases. Thus, it is necessary to figure out an energy-efficient method to improve thermal robustness of optical interconnects with on-chip lasers.

- **Architecture**

  Different communication schemes and resource assignments in architectures contribute differently to the worst-case optical loss, even in the same topology and layout. Given that lower worst-case loss of communication is advantageous for the overall energy efficiency, an architecture needs to be designed based on the topology and layout exploration.
2.6. References


Chapter 2 State of art of silicon photonic interconnects on chip


Chapter 2 State of art of silicon photonic interconnects on chip


Chapter 3. Passive topology and layout guidelines

Decreasing the worst-case loss is mandatory to reduce the overall system power consumption. The major sources of losses consist of signal propagation in waveguides, waveguide crossings and MR drop. The reduction of losses can be achieved by: i) improving the network topology; ii) optimizing the layout; and iii) using new fabrication process such as multi-layer silicon deposited technology.

In this chapter, we first present topologies of the popular optical crossbars in Section 3.1. Then, physical layouts for both single-layer and multi-layer implementations of the considered crossbars are presented in Section 3.2 and Section 3.3, respectively. In Section 3.4, the optical loss model is presented and the methodology to evaluate the worst-case loss is proposed. In Section 3.5, the evaluation results of the single-layer and multi-layer implementations are provided. Finally, the conclusion of this chapter is given in Section 3.6.

3.1. Popular optical crossbar topologies

3.1.1. Topology summary

Numerous silicon photonic interconnects relying on WDM have been proposed. In addition, wavelength routing scheme can be used to propagate data from a source IP core to a destination IP core, leading to a contention-free network, so called WRONoC (i.e., wavelength routed ONoC). Thus, without the need of arbitration, optical crossbars based on wavelength routing scheme become popular, with the property of high throughput and low latency.

The crossbar topologies considered in this work are: Matrix [3], λ-router [4], Snake [5], and ORNoC [6], as shown in Figure 24. In the figure, each column is dedicated to a topology and the rows show their i) structural views and ii) implementation characteristics. We briefly introduce these topologies and illustrate the way they can be used to interconnect 2×2 IP cores. We also evaluate the number of required optical devices, assuming $N$ is an even number. $N_{MR}$, $N_{MR, det}$, $N_{laser}$ and $N_{wl}$, represent the number of MRs in the network itself after the reduction, the number of MRs in the receiver interface, the number of laser sources, and the number of wavelengths. In this work, we consider fully connected optical crossbars.
### 3.1.2. Matrix

Figure 24-a illustrates a simple example where 4 IP cores are interconnected using Matrix. Full connectivity is considered, which leads to a total of 16 MRs in this example. By considering only inter-IP core communications, one MR per line of the Matrix can be removed. Thus, for \( N \times N \) IP cores, \((N^2 - 1) \times N^2\) passive MRs are used to implement the crossbar itself. The transmitters are composed of on-chip laser sources [1], and the receivers are composed of photodetectors and passive MRs that drop the signal into the photodetector (not illustrated in the figure for the sake of clarity). Because we focus on crossbar networks, we assume dedicated communication between all the IP cores through spatial WDM. As a consequence, \((N^2 - 1) \times N^2\) laser sources, with the same number of photodetectors and passive MRs, are required in the network interface. It is worth noticing that all topologies considered in this work require the same number of laser sources and photodetectors. Matrix topology uses \((N^2 - 1)\) wavelengths to implement all the communications.

### 3.1.3. \(\lambda\)-router

\(\lambda\)-router is a multistage network topology relying on WDM and wavelength routing to propagate optical signals from input to output ports. Compared to the Matrix, the multistage structure allows reducing the number of waveguide crossings in the worst-case scenario (6 and 3,
for Matrix and λ-router, respectively, in the case of 4 IP cores). This is achieved by assuming symmetric 2×2 switches structure relying on 2 identical MRs.

3.1.4. **Snake**

Snake is, also, a multistage network topology. It has the same properties with the λ-router. The only difference is the distribution of the MRs in the network, which leads to the more compact layout compared to λ-router, with the side effect of different waveguide lengths between different input and output pairs.

3.1.5. **ORNoC**

In ORNoC, the inter-IP core communication is realized through waveguides forming a ring. The following operations are performed:

- **Injection**: the IP core injects an optical signal into a waveguide through its output port. The wavelength of the signal specifies the destination of the IP core;
- **Pass through**: the incoming signal propagates along the waveguide (i.e., no MR with the same resonant wavelength is located along the waveguide);
- **Ejection**: the incoming optical signal is ejected from the waveguide and redirected to the destination IP core. This is achieved by an MR located along the waveguide at the same resonant wavelength with the signal.

In ORNoC, the same wavelength can be used to realize multiple communications in the same waveguide at the same time, due to the partition of the ring. Furthermore, multiple waveguides can be used to interface IP cores. Both clockwise (C) and counter-clockwise (CC) directions can be considered for signal propagation, where each direction is realized in a separate waveguide. For this comparative study, we consider two versions of ORNoC: ORNoC\(_C\) and ORNoC\(_C-CC\), relying on only the C direction, and both C and CC directions, respectively. They are illustrated in Figure 24-d1 and -d2 separately: blue and red lines represent C and CC directions. Compared to the other networks, no MR is used in the network itself (i.e., MRs are used only in the network interfaces), which leads to a reduction of the total number of optical devices. However, the ring structure implies crossing intermediate network interfaces, which leads to an increase of the minimum number of wavelengths to be used (e.g., 6 and 3 wavelengths are required to interconnect 4 IP cores with ORNoC\(_C\) and ORNoC\(_C-CC\), respectively).
3.2. **Single-layer Layouts**

For the popular optical crossbar topologies, we name the corresponding single-layer implementations as Matrix\textsubscript{SL}, \(\lambda\)-router\textsubscript{SL}, Snake\textsubscript{SL}, and ORNoC\textsubscript{SL}. On-chip laser sources are assumed for all the layouts since they do not lead to the use of power waveguides as with off-chip lasers, which contribute to reduced number of waveguide crossings and thus improve energy efficiency.

3.2.1. **Single-layer architecture**

Figure 25 illustrates the considered 3D architecture model. It consists of an electrical layer and an optical layer. The electrical layer is composed of IP cores which are uniformly arranged into an \(N\times N\) mesh, with \(N\) an even number (e.g., \(N=4\) in Figure 25). The IP cores process and store data, and the data among the cores are exchanged through an optical crossbar implemented by using the optical layer (ring topology in the example). The optical layer is composed of optical devices, such as on-chip lasers (e.g., VCSEL\textsuperscript{[1]}), waveguides, MRs, and photodetectors. The two layers are connected by using TSV\textsuperscript{[2]}. In our work, we assume \(N\) is an even number, but the work could be easily extended for odd values and for \(N\times M\) IP cores architectures.

![Figure 25: The optical crossbar (ring topology in the example) is implemented in the optical layer and it interconnects IP cores located in the electrical layer.](image)

Optical Network Interfaces (ONIs) enable the communication between IP cores through the optical layer. The optical part is used to propagate data and the electrical part is responsible for the control of the optical part. Each ONI is composed by receiver and transmitter parts. The receiver part can eject signals at a given set of wavelengths, while the transmitter part can inject signals with another set of wavelengths. The transmitter part is constituted by on-chip lasers (e.g., VCSELs\textsuperscript{[1]}) which emit optical signals, and MRs that couple the signals to the waveguide
which connects two neighboring ONIs. The receiver part is composed of passive MRs (i.e., always at ON state) and photodetectors. The MR drops the optical signal at the resonant wavelength from the waveguide. The dropped signal reaches a photodetector. Then, the photodetector detect the optical signal and convert it back to electrical domain. For instance, Figure 26 shows an ONI example for ring topology, in which electrical part is not shown for the sake of clarity.

![Diagram of an ONI in ring topology](image)

**Figure 26:** An example of ONI in ring topology.

### 3.2.2. Matrix\textsubscript{SL}

Figure 27-a and -b present two possible layouts: i) layout\textsubscript{w0x} and ii) layout\textsubscript{x}, which are respectively designed to i) avoid any waveguide crossing between the network interfaces and the crossbar network itself and ii) reduce the worst-case waveguide length between IP cores. For layout optimization purposes, the crossbar network is located in the middle of the optical layer, which also allows keeping a symmetrical structure (represented by a box for the sake of clarity in the figure). It interconnects 16 inputs (in red lines) with 16 outputs (in blue lines) through 240 MRs.

For each IP core, we consider that optical signals are injected and ejected on opposite sides of the interface (i.e., with the transmitter and the receiver part being located on the different sides of the interface). This allows: a) to keep the layout regular, b) to avoid the use of extra waveguide crossing and c) to reduce the waveguide length. In order to match with the layout constraints from the regular \(N\times N\) IP cores architecture, the transmitter and the receiver part of the IP cores are connected to the inputs and the outputs of the crossbar with waveguides, respectively. In this work, we consider only X and Y directions for the waveguides placing and routing, which simplifies the design rules, but can lead to extra waveguide length. The same layout rules will be assumed to interface with both \(\lambda\)-router and Snake networks.
Figure 27: Layout summary of considered optical crossbars: a) layout$^{\text{st}}_{\text{SL}}$ and b) layout$^{\text{st}}_{\text{SL}}$ for Matrix$_{\text{SL}}$, $\lambda$-router$_{\text{SL}}$, and Snake$_{\text{SL}}$, c1) ORNoC$_{\text{SL}}$ and c2) ORNoC$_{\text{SL}}^{\text{CC}}$.

### 3.2.3. $\lambda$-router$_{\text{SL}}$ and Snake$_{\text{SL}}$

The initial structure of $\lambda$-router would assume 240 MRs, for the architecture with 4$\times$4 IP cores, but a reduction method [4] reduces the network complexity by managing only the required optical connections and by removing the unused MRs. As a result, 224 MRs are required to implement the network.

Similarly to $\lambda$-router$_{\text{SL}}$, a reduction method adapted from [4] can be applied to remove the unused MRs in Snake$_{\text{SL}}$. The interconnect layouts for $\lambda$-router$_{\text{SL}}$ and Snake$_{\text{SL}}$ are the same with Matrix$_{\text{SL}}$: layout$^{\text{st}}_{\text{SL}}$ and layout$^{\text{st}}_{\text{SL}}$ in Figure 27-a and -b.

### 3.2.4. ORNoC$_{\text{SL}}$

Corresponding to ORNoC$_{\text{C}}$ and ORNoC$_{\text{CC}}$, two layouts are considered in Figure 27-c1 and -c2 respectively, i.e., ORNoC$_{\text{SL}}^{\text{C}}$ and ORNoC$_{\text{SL}}^{\text{CC}}$. 16 IP cores are connected by waveguides in either C or/and CC direction. Blue and red lines represent the waveguides in C and CC directions separately. If the number of wavelengths in one waveguide reaches the maximum, additional
waveguides can be added in order to realize all the communications. In this case, compared to other crossbar layouts, the serpentine layout in ORNoC$_{\text{SL}}^C$ and ORNoC$_{\text{CC}}^C$ enables no impact on layout complexity and waveguide crossings. This advantage can thus improve the energy efficiency by avoiding the increase of waveguide crossings.

### 3.3. Multi-layer layouts

In this section, multi-layer deposited silicon technology is used to reduce optical loss and thus improve energy efficiency. We name the corresponding multi-layer layouts as Matrix$_{\text{ML}}$, λ-router$_{\text{ML}}$, Snake$_{\text{ML}}$, and ORNoC$_{\text{ML}}$.

#### 3.3.1. Multi-layer architecture and devices

![Figure 28: The optical crossbar (ring topology in the example) is implemented in the optical layers and it interconnects IP cores.](image)

Figure 28 illustrates the considered 3D architecture model, by using an architecture example for 4x4 IP cores. Different from the single-layer implementation, two optical layers (ring topology for the optical interconnect in the example) are utilized and stacked on top of an electrical layer.

For layer 1, we assume a crystalline silicon (c-Si) waveguide, with a cross-section dimension of 500nm×220nm ($W \times H$) and a refractive index ($n_{\text{Si}}$) of 3.45. A reported propagation loss is 2.85dB/cm [11] and it has been reduced to 0.5dB/cm [9]. For layer 2, we assume a CMOS-compatible silicon nitride (Si$_3$N$_4$) waveguide, with a cross-section dimension of 1000nm×400nm ($W \times H$) and a refractive index ($n_{\text{Si3N4}}$) of 2. Reported propagation loss is 1.3dB/cm [11] around 1550nm and optimized implementations allow reducing the loss to 0.1dB/cm [9]. By using
silicon dioxide (SiO$_2$) as the cladding ($n_{SiO_2}=1.5$), high confinement of the optical signal and sharp bending radius are achieved.

![Diagram of one layer and two layers implementations](image.png)

**Figure 29: Implementations with one layer and two layers of: a) waveguide crossing, b) waveguide, c) MR, and d) PSE.**

Figure 29-a illustrates the top-view of a waveguide crossing implemented with a single-layer (which leads to 0.05-0.2dB loss) and with two layers (nearly 0dB losses when waveguides are placed orthogonally with an appropriate vertical gap [19]). The top-view of a waveguide designed with single-layer and multi-layer technologies are shown in Figure 29-b. In addition, 3D implementation of photonic devices is also possible. MRs [9] (Figure 29-c) and Photonic Switching Elements (PSEs) (Figure 29-d) can also be efficiently implemented by means of the multi-layer technology.
3.3.2. **Matrix\_ML**

Figure 30-a illustrates a multi-layer implementation of Matrix used to interconnect four cores. Waveguide crossing are avoided by allocating inputs and outputs waveguides on the first and the second layer respectively. For its implementation, Matrix uses 16 MRs to fully interconnect the 4 cores. The MRs located on the diagonal can be removed if only inter-core communications are considered, which leads to \((N^2-1)\times N^2\) MRs for \(N\times N\) cores architecture.

![Matrix ML diagram](image)

**Figure 30:** a) Matrix\_ML topology, b) layout without waveguide crossings (layout\_w/o\_ML) and c) layout with the shortest waveguide length (layout\_w\_ML).

In order to match with the layout constraints from regular \(N\times N\) architecture, Matrix is located in the middle of the optical layer for layout symmetry purposes, as illustrated in Figure 30-b and -c. The ONI transmitter part and receiver part must be connected to the Matrix input and output respectively. Achieving an optimal layout is not an easy task. It depends on system-level parameters (e.g., number of cores and distance between the cores) and technological parameters (e.g., insertion losses). For instance, if \(P_{\text{propagation}}\) is high (e.g., 2dB/cm), a layout with waveguide crossings but shorter waveguides may show lower total losses \(L_{\text{total}}\) than a layout without waveguide crossings but with longer waveguides. Therefore, for a fair comparison with ORNoC\_ML, which avoids waveguide crossings in the same layer, we assumed two layouts. The
first layout, shown in Figure 30-b, avoids waveguide crossings and is named Matrix_{ML}^{w/oX}. The second layout, shown in Figure 30-c, minimizes the waveguide length and is named Matrix_{ML}^{wX}.

3.3.3. $\lambda$-router_{ML} and Snake_{ML}

$\lambda$-router and Snake are multi-stage optical networks that can be implemented in similar way, as illustrated in Figure 31-a and -b. The optical signals propagate along the waveguides and are dropped from a waveguide to another, in order to reach the targeted outputs. The switching structure of $\lambda$-router and Snake is a symmetric PSE implemented with two identical MRs. The method proposed in [4] is also used: by managing only the required communications, the unnecessary PSEs are removed, which helps reducing the network complexity. By considering only inter-core communications, the PSEs located in the central row and the central column of $\lambda$-router and Snake are removed, respectively.

Multi-stage topologies lead to a significant number of waveguide crossings in the worst-case path. Indeed, for networks with $N$ inputs, there are $N^2-1$ and $2N^2-5$ waveguide crossings in the worst-case path of $\lambda$-router and Snake, respectively. This can be significantly reduced by assuming two-layer implementations illustrated in Figure 31-a and -b. For the sake of regularity and symmetry, the input waveguides are alternately located in the first and second layers. By using this layout design rule, for a 4x4 architecture size of $\lambda$-router and Snake crossbars, the number of waveguide crossings in the worst-case path is reduced from 15 and 27 to 12 and 13, respectively. It represents 20% and 51.9% reduction separately. PSEs with waveguides located in different layers are implemented as described in Figure 29-d.

Similarly to Matrix, the inputs and outputs of the network (located in the center of the optical layer) are connected to the ONIs assuming two layouts. The first layout, shown in Figure 31-c, avoids waveguide crossings and leads to $\lambda$-router_{ML}^{w/oX} and Snake_{ML}^{w/oX}. The second layout, shown in Figure 31-d, minimizes the waveguide length and corresponds to $\lambda$-router_{ML}^{wX} and Snake_{ML}^{wX}. The layouts will be compared in the result section of the paper.
3.3.4. ORNoC<sub>ML</sub>

3.3.4.1. Multi-layer implementation of ring based optical crossbar

ORNoC is a ring based optical crossbar [6][14] illustrated in the left-hand side of Figure 32. The main feature of ORNoC is the absence of waveguide crossings, which is possible due to the serpentine layout and the use of on-chip lasers. In the figure, solid and dot lines represent the clockwise (C) and counter-clockwise (CC) directions for signal propagations, respectively. The same wavelength can be used to realize multiple communications in the same waveguide at the same time, efficiently implementing Single-Write-Single-Read (SWSR) communication scheme.
This is possible only if the different communications do not have any overlapping paths. Furthermore, multiple waveguides can be used to transmit optical signal in C and CC directions.

ORNoCML is the multi-layer implementation of ORNoC and is illustrated in the right-hand side of Figure 32. It implements a second set of rings located on the second layer, with the aim to improve the connectivity between the IP cores thanks to reduced losses. Red and blue colors are used to represent waveguides located in the first and second layer, respectively. The ring layouts in the second layer are rotated by 90° compared to the first layer layout. Since the additional waveguides are located in a different layer, the propagation of signal does not suffer from any additional waveguide crossing loss.

![Figure 32: Optical crossbars ORNoCML and ORNoCML: a) topology to interconnect 9 IP cores and b) layout for 4x4 IP cores.](image)

The following illustrates the advantages of ORNoCML over ORNoC, assuming the same propagation loss value for both layers for the sake of clarity. The left-hand side of Figure 32-b shows the single-layer ORNoC layout for 4x4 cores. In order to perform the communication with
the lowest $L_{propagation}$ between the $IP_1 \rightarrow IP_9$ and $IP_4 \rightarrow IP_2$, the C and CC directions are employed, respectively. Note that the response communications (i.e., $IP_9 \rightarrow IP_1$ and $IP_2 \rightarrow IP_4$) will be performed in opposite directions, i.e., by using CC and C. $IP_1 \rightarrow IP_9$ is one of the communication paths that experience the most losses. Single-layer ORNoC implementation requires the crossing of 7 intermediate interfaces. By considering a mesh distribution of the interfaces and a distance $d$ between neighboring IP cores, the total propagation distance is thus $8d$. In order to reduce this distance, dedicated waveguide for $IP_1 \rightarrow IP_9$ can be integrated in the same layer (e.g., $IP_1 \rightarrow IP_2 \rightarrow IP_3 \rightarrow IP_6 \rightarrow IP_9$). However, this will: i) introduce waveguide crossings; and ii) affect the regularity, thus leading into a less scalable network. With ORNoC$_{ML}$, $IP_1 \rightarrow IP_9$ and $IP_9 \rightarrow IP_1$ are implemented on the second layer by using C and CC directions since the propagation distance is shorter than that in the first layer. Communications between $IP_2 \rightarrow IP_4$ and $IP_4 \rightarrow IP_1$ are still implemented in the first layer. Hence, ORNoC$_{ML}$ avoids the introduction of additional waveguide crossings and reduces the propagation distance, while keeping the layout regular.

![Figure 33: An Optical Network Interface.](image)

Figure 33 illustrates a layout example for an ONI in ORNoC$_{ML}$. The waveguides in red and blue allow the propagation of optical signals in the first and second layer, respectively. In this example, a single waveguide is considered. However, multiple waveguides can be regularly implemented without any waveguide crossing by applying the layout guidelines from [6]. Communications occurring on layer 1 will be achieved as in the single layer implementation of ORNoC. The signal propagating on the second layer will cross two OVCs: the first vertical
coupling will occur right after their emission by the laser (i.e., layer 1 → layer 2) and the second coupling will occur just before their reception by the photodetector (i.e., layer 2 → layer 1).

3.3.4.2. Design method

ORNOC\textsubscript{ML} is designed following a two-step methodology. First, each communication is assigned to the ring (i.e., layer/direction couple) minimizing the total loss. Then, for each ring, wavelengths are assigned to the communication following an iterative algorithm. The following details the method.

3.3.4.2.1. First step: ring assignment

In the first step, we select, for each communication, the optical path with the lowest propagation losses. For this purpose, four distance matrixes are computed, each for one possible ring implementation (i.e., layer 1/2 and direction C/CC). Each communication is assigned to the layer-direction couple showing the shortest distance.

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline
D  & IP₁ & IP₂ & IP₃ & IP₄ & IP₅ & IP₆ & IP₇ & IP₈ & IP₉ & IP₁₀ & IP₁₁ & \ldots \\
\hline
IP₁ & - & C & C & C & C & CC & CC & C & C & CC & CC & \ldots \\
IP₂ & CC & - & C & C & CC & C & CC & C & C & CC & CC & \ldots \\
IP₃ & CC & CC & - & C & CC & C & C & CC & C & CC & CC & \ldots \\
IP₄ & CC & CC & CC & - & CC & C & C & CC & C & CC & CC & \ldots \\
\vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \ldots \\
IP₉ & CC & CC & C & C & - & C & C & \ldots & \ldots & \ldots & \ldots & \ldots \\
IP₁₀ & C & CC & CC & CC & CC & CC & - & C & \ldots & \ldots & \ldots & \ldots & \ldots \\
IP₁₁ & C & C & CC & CC & CC & CC & CC & - & \ldots & \ldots & \ldots & \ldots & \ldots \\
\vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \ldots \\
\hline
\end{tabular}
\caption{Ring assignment matrix for 4x4 IP cores.}
\end{table}

Figure 34 illustrates an excerpt of the ring assignment for the 4x4 architecture illustrated in Figure 32, assuming the same propagation loss value for layer 1 and layer 2. Source and destination IP cores are represented in column and row, respectively. In this example, all the communications between IP₁, IP₂, IP₃ and IP₄ use the rings located on the first layer. Some communications will use C ring (e.g. IP₁→IP₂) and the others CC (e.g., IP₂→IP₁). As another example, IP₁→IP₉ and IP₉→IP₁ are implemented by using layer 2 in C and CC directions,
respectively. In case the distances on layer 1 and layer 2 are the same, layer 1 is used in order to avoid vertical couplers. The wavelength assignment in each ring is achieved in the second step.

3.3.4.2.2. Second step: wavelength assignment algorithm

The design of ORNoC<sub>ML</sub> requires careful wavelength assignment between cores in order to reduce the number of wavelengths and the number of waveguides per direction. Additional waveguides must be included if the maximal number of wavelengths is reached in a waveguide. From ring assignment obtained in the first step, the wavelengths are assigned as follow. For each ring, an initial IP source \( IP_i \) and wavelength \( wl_i \) is defined. Then, \( wl_i \) is assigned to the longest optical path from \( IP_i \), which allows reaching destination \( IP_d \). The operation is repeated from \( IP_d \), until \( IP_i \) is reached (i.e., wavelength \( wl_i \) has been assigned on all the segments of the waveguide). Another wavelength is used and the assignment process is repeated until a wavelength has been assigned to all the communications from \( IP_i \). Then, a new wavelength is used and the process restarts from the following IP, etc. If the wavelengths number reaches the maximum value allowed per waveguide, a waveguide is added and the algorithm continues its execution from the initial wavelength. For symmetry purpose, bidirectional communications (i.e., communications occurring on a same layer but in opposite directions) are implemented with the same wavelength.

3.4. Worst-case loss evaluation methodology

The minimum laser output power, required to complete a communication, depends on the total loss along the optical path from the source IP core to the destination IP core, together with the receiver sensitivity under a given BER. That is to say, higher losses will require higher minimum laser output power, resulting in lower energy efficiency in the silicon photonic interconnects. Therefore, the worst-case and average losses are key metrics to estimate the energy efficiency. In this section, the optical loss model used to evaluate the different architectures is introduced firstly. Then the worst-case loss evaluation methodology is illustrated.

3.4.1. Optical loss model

Figure 29 presents the losses parameters we assume and the total loss along an optical path \( L_{total} \) is given in equation (3.1). \( L_{total} \) depends on: i) the total propagation loss in the waveguide \( L_{propagation} \), given by (3.2) and represented in Figure 29-b; ii) the total loss due to the effective number of waveguide crossings \( L_{crossing} \) given by (3.3) and represented in Figure 29-a; iii) the
total drop loss $L_{\text{drop}}$ given by (3. 4) and represented in Figure 29-c and -d; iv) the coupler loss $L_{\text{OVC}}$ given by (3. 5) and represented in Figure 29-b; v) the total through loss $L_{\text{through}}$ when a signal passes by a non-resonant MR; and vi) the waveguide bending loss $L_{\text{bending}}$. In this work, we assume $P_{\text{bending}} = 0.005\text{dB}/90^\circ$ [9] and $L_{\text{through}}$ is neglect. We also assume negligible crosstalk between waveguides, which can be obtained by considering a 5µm distance between parallel waveguides. Indeed, for 5mm parallel waveguides assuming $500\text{nm} \times 220\text{nm} (W \times H)$, the power coupling between the waveguides will be lower than $-40\text{dB}$, when the gap side by side is 3 µm or more [12]. The loss induced by the fabrication process variation is not considered in this work. The parameters used in the formulation are detailed in Table 3 and Table 4.

$$L_{\text{dB}} = L_{\text{propagation}}^\text{dB} + L_{\text{crossing}}^\text{dB} + L_{\text{drop}}^\text{dB} + L_{\text{through}}^\text{dB} + L_{\text{bending}}^\text{dB} + L_{\text{OVC}}^\text{dB} \quad (3.1)$$

$$L_{\text{propagation}} = P_{\text{propagation},1} \times l_{s-d,1} + P_{\text{propagation},2} \times l_{s-d,2} \quad (3.2)$$

$$L_{\text{crossing}} = P_{\text{crossing}} \times N_{\text{crossing}} \quad (3.3)$$

$$L_{\text{drop}} = P_{\text{drop},1} \times N_{\text{drop},1} + P_{\text{drop},2} \times N_{\text{drop},2} \quad (3.4)$$

$$L_{\text{OVC}} = P_{\text{OVC}} \times N_{\text{OVC}} \quad (3.5)$$

From the total loss along a communication path between any pair of source/destination IP cores (shown in equation (3. 1)), the worst-case loss ($L_{\text{wc}}$) and the average loss ($L_{\text{avg}}$) are estimated by using equation (3. 6) and (3. 7). In these equations, $L$ is the set of total losses (i.e., $L_{\text{total}}$ in equation (3. 1)) for all the communication paths in the network. This model is generic and can be used for both single-layer and multi-layer implementations. For the single-layer implementation, the losses only take place in one layer (i.e., layer 1) and the coupler loss does not exist.

$$L_{\text{wc}} = \text{Maximum}(L) \quad (3.6)$$

$$L_{\text{avg}} = \text{Average}(L) \quad (3.7)$$

From the worst-case loss ($L_{\text{wc}}$) and the receiver sensitivity ($OP_{\text{sensitivity}}$), the required minimum laser output power ($OP_{\text{min_laser}}$) under a given BER can be obtained by using equation (3. 8):

$$OP_{\text{min_laser}}^\text{dBm} = L_{\text{wc}}^\text{dB} + OP_{\text{sensitivity}}^\text{dBm} \quad (3.8)$$
### Table 3: Insertion Loss Parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>$P_{\text{propagation},1}$ (dB/cm)</td>
<td>Intrinsic propagation loss of waveguide in layer 1</td>
</tr>
<tr>
<td>$P_{\text{propagation},2}$ (dB/cm)</td>
<td>Intrinsic propagation loss of waveguide in layer 2</td>
</tr>
<tr>
<td>$P_{\text{crossing}}$ (dB)</td>
<td>Waveguide crossing loss</td>
</tr>
<tr>
<td>$P_{\text{drop},1}$ (dB)</td>
<td>Drop loss in the same layer</td>
</tr>
<tr>
<td>$P_{\text{drop},2}$ (dB)</td>
<td>Drop loss in MR and PSE in different layers</td>
</tr>
<tr>
<td>$P_{\text{OVC}}$ (dB)</td>
<td>Vertical coupling loss (in OVC)</td>
</tr>
</tbody>
</table>

### Table 4: Network Implementation Characteristics.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$l_{s,d,1}$</td>
<td>Waveguide length between a source and a destination in layer 1</td>
</tr>
<tr>
<td>$l_{s,d,2}$</td>
<td>Waveguide length between a source and a destination in layer 2</td>
</tr>
<tr>
<td>$N_{\text{crossing}}$</td>
<td>Number of waveguide crossings</td>
</tr>
<tr>
<td>$N_{\text{drop},1}$</td>
<td>Number of intra-layer drop operations</td>
</tr>
<tr>
<td>$N_{\text{drop},2}$</td>
<td>Number of inter-layer drop operations</td>
</tr>
<tr>
<td>$N_{\text{OVC}}$</td>
<td>Number of vertical couplers along a path</td>
</tr>
</tbody>
</table>

For instance, in the single-layer implementation, the waveguide length between the source and destination $l_{s,d}$ depends on the layout represented in Figure 27. The key metrics to evaluate $L_{\text{waveguide}}$, $L_{\text{crossing}}$, and $L_{\text{drop}}$ are $l_{s,d}$, $N_{\text{crossing}}$, and $N_{\text{drop}}$. For Matrix, $\lambda$-router and Snake networks, both layouts (i.e., layout $w/o X_{\text{SL}}$ and layout $X_{\text{SL}}$) are considered, which leads to: bigger longest waveguide length in layout $w/o X_{\text{SL}}$, and more additional waveguide crossings in layout $X_{\text{SL}}$. We do not consider the distance between inputs and outputs of the network itself. For all aforementioned networks, two drop operations occur: one in the network itself, and the other one in the receiver interface to drop the signal into the photodetector.

Both ORNoC$^{C}_{\text{SL}}$ and ORNoC$^{C,CC}_{\text{SL}}$ do not suffer from any waveguide crossing and the signal is dropped only once in the receiver part ($N_{\text{crossing}}=0$ and $N_{\text{drop}}=1$). However, the considered serpentine layout implies that $l_{s,d}$ increases more rapidly when compared to the other networks. It is worth noticing that $l_{s,d}$ is significantly reduced for the C-CC case compared to the C case. This will result in a lower worst-case loss, which directly contributes to the energy-efficiency of ORNoC$^{C,CC}_{\text{SL}}$, as detailed in the results section.
3.4.2. Loss evaluation methodology

The worst-case loss $L_{\text{wc}}$ is evaluated by following the methodology illustrated in Figure 35 (single-layer implementation example). Considering both technological and structural values, which are related to the fabrication process and the network topology, enables a fair comparison of networks.

**Figure 35: The worst-case evaluation methodology of ONoCs.**

- The inputs of the methodology (Figure 35-a) are: i) the network topology, ii) the considered layout, and iii) the set of insertion loss values. In the example illustrated in
Figure 35, we consider a 2x2 Snake network topology, the layout assuming shortest waveguide length and insertion losses values from Biberman [9].

- The structural view of the resulting implementation is represented in Figure 35-b. Each communication between IP cores is divided into three routing parts: i) routing from the transmitter part of IP cores to the input of the network (represented with red lines), ii) routing in the network itself, and iii) routing from the output of the network to the receiver part of IP cores (represented with blue lines). Each link between an IP core output/input and a network input/output is represented with red/blue lines, respectively. It is characterized according to a) the number of the length $d$, b) the number of waveguide crossings, and c) the number of the drop operations, represented as a triplet $[a, b, c]$. For instance, the link from IP$_4$ to input 4 of the network is characterized by $[1, 2, 0]$, meaning that the length is $d$, there are 2 waveguide crossings, and no drop operation.

- From this structural representation, three matrices are generated: $M_{li}$, $M_n$, and $M_{lo}$ (Figure 35-c). They correspond to the three above mentioned routing parts. Regarding the matrix characterizing the network, $M_n$, no values correspond to in the diagonal, since only inter-IP core communications are considered.

- Based on $M_{li}$, $M_n$, and $M_{lo}$, a single matrix named $M_{ONoC}$ is obtained according to equation (3.9), as illustrated by Figure 35-d. This matrix represents each IP core to IP core communication using a triplet consisting of the total propagation distance of signals, the number of waveguide crossings, and drop operations.

$$M_{ONoC} = M_{li} \cdot \left[ \begin{array}{ccc} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{array} \right] + M_n \cdot \left[ \begin{array}{c} 1 \\ 0 \\ 1 \end{array} \right] \circ \left[ \begin{array}{cccc} 0 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 \\ 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 \end{array} \right]$$

(3.9)

- From the given set of insertion loss values (Figure 35-a) and $M_{ONoC}$ representation, the loss for each pair of the IP core communication is obtained by applying the equation (3.1), as illustrated in Figure 35-e.

Finally, the worst-case loss ($L_{wc}$) in the network is extracted by identifying the maximum value in the table (highlighted in red in the figure). The mean value of the communications gives the average loss ($L_{avg}$).
This methodology is generic enough to address any $N \times N$ network size. Moreover, the principle of the evaluation methodology can be applied to multi-layer implementation, even though the illustration is based on the single-layer implementation.

### 3.5. Results

#### 3.5.1. Single-layer implementation

We compare the topologies and corresponding single-layer layouts according to the worst-case and average losses. In a first comparison, all the related networks with two layouts (Matrix$_{wX}^{w/oX}$, Matrix$_{SL}^{wX}$, $\lambda$-router$_{SL}^{w/oX}$, $\lambda$-router$_{SL}^{wX}$, Snake$_{SL}^{w/oX}$, Snake$_{SL}^{wX}$) and ORNoC (ORNoC$_{SL}^{C \cdot C}$ and ORNoC$_{SL}^{C \cdot C}$) are considered by assuming a given set of technological values extracted from Table 5. In a second comparison, we further compare the networks assuming various design parameters.

#### Table 5: Insertion Loss Parameters

<table>
<thead>
<tr>
<th>Optical loss</th>
<th>$P_{crossing}$ (dB)</th>
<th>$P_{propagation}$ (dB/cm)</th>
<th>$P_{drop}$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pan [7]</td>
<td>0.05</td>
<td>1</td>
<td>1.5</td>
</tr>
<tr>
<td>Kirman [8]</td>
<td>0.12</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Biberman [9]</td>
<td>0.05</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Koka [10]</td>
<td>0.2</td>
<td>0.1</td>
<td>1.5</td>
</tr>
</tbody>
</table>

#### 3.5.1.1. Worst-case and average losses evaluation

We first assume a fixed 4cm$^2$ die size, and evaluate the losses for different architecture sizes: 2x2, 4x4, 6x6 and 8x8, where the distance between IP cores decreases as the number of IP cores increases, i.e., $d=10$mm, 5mm, 3.33mm and 2.5mm, respectively. Figure 36-a and -b illustrate the evaluation results for worst-case losses with the parameter values given by Pan [7] and Biberman [9], respectively.

We compare different layouts for Matrix, $\lambda$-router and Snake topologies using the values from Pan, as shown in Figure 36-a, where, for example Matrix$_{SL}^{w/oX}$ refers to Matrix topology in layout$_{SL}^{w/oX}$. It can be seen that the layout$_{SL}^{wX}$ outperforms layout$_{SL}^{w/oX}$ for 2x2 to 6x6 network sizes, but layout$_{SL}^{w/oX}$ shows better scalability, since the loss, especially the propagation loss, is less influenced by the increase of the IP number. For an architecture of 8x8 IP cores, layout$_{SL}^{w/oX}$ exhibits lower losses for Matrix and Snake. By considering values from Biberman (Figure 36-b), the same conclusion can be made for architectures containing up to 4x4 IP cores. However, for architectures with 6x6 and 8x8 IP cores, the worst-case loss is lower for layout$_{SL}^{w/oX}$, due to the
lower propagation loss in the waveguide, thus again highlighting the better scalability of this layout. From the comparison results in Figure 36-a and -b, ORNoC$^{CC}$ is the most scalable network despite the long waveguide length introduced by the serpentine layout. By considering values from Biberman, ORNoC$^{CC}$ is the most scalable network, with 4.5dB in the worst-case path for the architecture with 8x8 IP cores, followed by $\lambda$-router$^w$SL with 7.65dB, thus achieving 41.2% improvement compared to $\lambda$-router$^w$SL. By assuming parameters from Koka (not shown in the results), the worst-case loss in ORNoC$^{CC}$ and $\lambda$-router$^w$SL become 2.3dB and 16.3dB, respectively, thus leading to a 85.9% improvement for ORNoC$^{CC}$ over $\lambda$-router$^w$SL. Because of the rather large distance implied by the die size considered here, ORNoC$^C$ does not exhibit as good scalability as ORNoC$^{CC}$.

Figure 36: Worst-case losses evaluation for 2x2 to 8x8 IP cores assuming insertion loss parameters from a) Pan [7] and b) Biberman [9].

Figure 37 shows results of the average loss comparison. Compared with all the implementations of Matrix, $\lambda$-router and Snake (i.e., using both layouts), ORNoC$^{CC}$
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demonstrates, on average, 46% and 56% reduction of the losses by considering Pan and Biberman values, respectively. This is achieved by avoiding the waveguide crossings in the serpentine layout, and by reducing the signal propagation distance thanks to the use of both C and CC directions. For 8x8 IP cores and by considering the value set from Biberman, the improvement over Snake\textsubscript{wX}SL reaches 69% (ORNoC\textsubscript{C,CC}SL and Snake\textsubscript{wX}SL demonstrate 2.5dB and 8dB, respectively). Moreover, thanks to this reduction in the average loss, additional significant power reduction can be achieved by considering the use of tunable lasers output power.

![Graph](image)

**Figure 37:** Average losses evaluation for 2x2 to 8x8 IP cores assuming insertion loss parameters from a) Pan [7] and b) Biberman [9].

Figure 38 represents the worst-case loss for a fixed size of 6x6 IP cores, and various distances between them (i.e., d=1, 1.5, 2, 2.5 and 3mm) by assuming insertion loss parameters given by Pan [7] and Biberman [9], separately. The impact of the distance increase is higher for the networks relying on layout\textsubscript{wX}SL than layout\textsubscript{wX}SL. The relative increase of the loss with the distance is the greatest for ORNoC\textsubscript{C}SL and ORNoC\textsubscript{C,CC}SL, due to the serpentine layout. Still, even for
a 3mm distance, which implies a realistic 3.24cm² die size, ORNoC\textsuperscript{C-CC}_{SL} remains the most power-efficient network for both sets of the insertion loss parameters.

Figure 38: Evaluation of the impact of the distance between IP cores in size of 6x6 on the worst-case losses assuming insertion loss parameters from a) Pan [7] and b) Biberman [9].

3.5.1.2. Implementation comparison

In order to further explore the design space, we observe the example of a set of architectures with 6x6 IP cores, and various distances d (in the range of 1mm-3mm with 0.5mm increments). We consider a range of 0-2dB for propagation loss and a range of 0-0.15dB for waveguide crossing loss. Figure 39 illustrates comparison results for the implementations of \( \lambda \)-router with both layout\textsuperscript{w/oX}_{SL} (i.e., without waveguide crossing) and layout\textsuperscript{X}_{SL} (i.e., with shorter waveguide length), by assuming \( P_{\text{drop}}=1\text{dB} \). We also plot the values for \((P_{\text{crossing}}, P_{\text{propagation}})\) from Table 5. The area below each line represents the design space for which the worst-case loss is lower for layout\textsuperscript{w/oX}_{SL}; the area above the line gives the design space where the worst-case loss is lower for layout\textsuperscript{X}_{SL} and the line itself represents the designs with the same worst-case losses for both
layouts. For example, layout \( w_{\text{SL}}^{w/oX} \) shows lower worst-case loss for the values from Pan [7], Biberman [9], Kirman [8] when the distance is smaller than or equal to 1.5 mm. In addition, the result indicates that layout \( w_{\text{SL}}^{w/X} \) performs better as the distance gets smaller, since the loss is less impacted by the waveguide propagation. Overall, this further helps to determine the most appropriate layout for a given set of insertion loss values and a given distance between IP cores.

![Graph comparing optical loss values](image)

**Figure 39: Comparison of \( \lambda\)-router\( w_{\text{SL}}^{w/X} \) and \( \lambda\)-router\( w_{\text{SL}}^{w/X} \) (6x6 IP cores, \( P_{\text{drop}}=1 \text{dB} \)).**

These comparisons highlight the importance of technological parameters, layout and network topology to evaluate the worst-case optical loss. We can see that for a given set of technological values (e.g., crossing loss and propagation loss), certain topology and layout may be more advantageous, which may significantly impact the overall power efficiency of the crossbar.

### 3.5.1.3. Designing complexity comparison

For a fair comparison of the considered optical crossbars, we also evaluate their implementation complexity while interconnecting \( N^2 \) IP cores. We compare implementation complexity using the numbers of the required MRs and waveguides.

The number of MRs is an important metric since it affects the network scalability. In general, with increase in the number of the IP cores, the number of the MRs also increases. It is worth noticing that all the networks require the same number of the lasers and photodetectors, and that one MR per photodetector is required in the interface. As a consequence, we only evaluate the number of MRs inside the network itself. The implementation of Matrix network requires \( (N^2-I)\times N^2 \) MRs, which is slightly higher than the number required by \( \lambda\)-router and Snake \( ((N^2-2)\times N^2) \).
ORNoC does not require any MRs in the network, which leads to a lower design complexity, and, therefore, better scalability.

In ORNoC, the number of waveguides required for the implementation depends on the maximum number of wavelengths per waveguide. Indeed, ORNoC$_{SL}$ (respectively ORNoC$_{CC}$) requires $(N^2-1)xN^2/2$ (respectively $(N^2-1)xN^2/4$) waveguides, assuming a single wavelength per waveguide. By considering $N^2$ possible wavelengths per waveguide (i.e., the number of wavelengths required by both λ-router and Snake), the number of the required waveguides for the implementation of ORNoC$_{CC}$ is reduced to $(N^2-1)/2$ (resp. $(N^2-1)/4$). Hence, for the same number of wavelengths, both implementations of ORNoC require fewer waveguides compared to Matrix $(2N^2)$, λ-router $(N^2)$ and Snake $(N^2)$. For example, for a 8x8 architecture with a single waveguide per direction, ORNoC$_{CC}$ requires 1008 wavelengths in one waveguide compared to 63 wavelengths for Matrix and 64 for Snake and λ-router. 1008 is not a realistic value with regard to the number of wavelengths. Following the methodology from [6], ORNoC would require 16 waveguides if we consider a maximum number of 64 wavelengths per waveguide, while Matrix, λ-router and Snake, would require 128, 64 and 64 waveguides, respectively. This also contributes to the lower design complexity and the better scalability. In addition, when the network size increases, there is a need for increasing number of the waveguides and wavelengths for implementation of optical crossbars. If a constraint such as the maximum number of wavelengths per waveguide (with optimistic value of 64) must be respected for all the considered networks, Matrix, λ-router and Snake could satisfy the constraint by considering the use of multiple networks, which implies additional waveguide crossings [16]. However, it is important to notice that additional waveguides can be used in ORNoC$_{CC}$ to satisfy the given constraint, and this can be achieved without any waveguide crossing because of the 3D architecture and the use of on-chip laser sources. Moreover, the layout of ORNoC$_{CC}$ is regular, and its $l_{s,d}$ is reduced compared to ORNoC$_{SL}$, which makes the network implicitly scalable without need for a custom place-and-route tool such as in [17][5][20].

3.5.2. Multi-layer implementation

We evaluate and compare the multi-layer implementations of the optical crossbars according to the worst-case loss and average loss metrics. We first discuss the technology related values to be used for the comparisons. In Section 3.5.2.2 and 3.5.2.3, we compare the best networks (i.e.,
Matrix\textsubscript{ML} and ORNoC\textsubscript{ML}) by exploring system-level and technology-level parameters. Also, we evaluate the laser power saving achieved thanks to the multi-layer based implementation of the optical crossbars. Finally, we give a summary of the results and we discuss the results.

### 3.5.2.1. Design parameters

#### Table 6: Insertion Loss Values

<table>
<thead>
<tr>
<th>Source IP core</th>
<th>$P_{\text{propagation,1}}$ (dB/cm)</th>
<th>$P_{\text{propagation,2}}$ (dB/cm)</th>
<th>$P_{\text{src}}$ (dB)</th>
<th>$P_{\text{drop,2}}$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Biberman [9]</td>
<td>0.5</td>
<td>0.1</td>
<td>0.1</td>
<td>0.6</td>
</tr>
<tr>
<td>Huang [11]</td>
<td>2.85</td>
<td>1.3</td>
<td>0.2</td>
<td>0.7</td>
</tr>
</tbody>
</table>

#### Figure 40: Ring assignment in ORNoC\textsubscript{ML} by assuming losses values from a) Biberman [9] and b) Huang [11].

We consider the insertion losses parameters from Biberman [9] and Huang [11] (Table 6), by assuming c-Si for layer 1 and Si\textsubscript{3}N\textsubscript{4} for layer 2. For both layers, $P_{\text{crossing}}=0.05\text{dB}$ and $P_{\text{drop,1}}=0.5\text{dB}$. For the multi-layer implementations of $\lambda$-router, Snake and Matrix, we evaluate the worst-case and average losses for each communication path following equation (3.1). This is achieved by evaluating four parameters: i) the signal propagation distance in both layers ($l_{s-d,1}$, $l_{s-d,2}$); ii) the number of waveguide crossing ($N_{\text{crossing}}$); iii) the drop operation ($N_{\text{drop,1}}$, $N_{\text{drop,2}}$); and iv) the inter-layer coupling ($N_{\text{src}}$). Regarding ORNoC\textsubscript{ML}, we follow the design method defined in Section 3.3.4.2 for the two sets of parameters. For a 4x4 architecture, the ring assignments obtained for Biberman and Huang parameters are given in Figure 40 -a and -b respectively. In both cases, most of the communications are allocated to layer 2 since it leads to the lowest...
propagation losses (0.1dB/cm w.r.t. 0.5dB/cm in Figure 40-a; 1.3dB/cm w.r.t. 2.85dB/cm in Figure 40-b). In Figure 40-a, slightly more communications are allocated to layer 1 (17.5%) compared to Figure 40-b (12.5%), which is due to smaller vertical coupling losses. This demonstrates the ability of our design method to assign communications on layer and direction according to technological parameters.

3.5.2.2. Crossbar comparison under system-level parameters exploration

3.5.2.2.1. Architecture sizes

We assume a fixed 2cmx2cm die size as in [15] and we evaluate the losses for 2x2, 4x4, 6x6 and 8x8 architecture sizes, i.e., distance between neighboring IP cores $d=10, 5, 3.33$ and $2.5mm$, respectively. All the results of this section are given for technological parameters from Biberman [9] (listed in Table 6).

In Figure 41, we first estimate the worst-case and average loss reductions (in %) for the two-layer implementation over the single-layer implementation for $\text{Matrix}_{w/X}^\text{ML}$, $\text{Matrix}_w^X$, $\lambda$-router$_{w/X}^\text{ML}$, $\lambda$-router$_w^X$, $\text{Snake}_{w/X}^\text{ML}$ and $\text{Snake}_w^X$ crossbars. 0% means that multi-layer and single-layer implementations lead to the same losses. Results above 0% indicate a reduction of the losses for the multi-layer implementation. Figure 41-a shows that improvements are obtained even for the smallest size architecture: the reduction of waveguide crossings allows compensating the vertical coupling losses. For instance, slight reduction of worst-case losses is obtained for 2x2 architecture size: $\text{Matrix}_{w/X}^\text{ML}$ (31%), $\text{Matrix}_w^X$ (24%), $\lambda$-router$_{w/X}^\text{ML}$ (4%), $\lambda$-router$_w^X$ (11%), $\text{Snake}_{w/X}^\text{ML}$ (4%) and $\text{Snake}_w^X$ (11%). For 8x8 size, the improvements of $\text{Matrix}_{w/X}^\text{ML}$, $\lambda$-router$_{w/X}^\text{ML}$ and $\text{Snake}_w^X$ reach 69%, 28% and 42%, respectively. The improvement for Snake is higher than for $\lambda$-router due to the initially higher number of waveguide crossings. Overall, Matrix demonstrates better improvement compared to $\lambda$-router and Snake since there is no additional waveguide crossings. The layout with the shortest waveguide length shows better improvement since it directly takes benefits from the reduction of the number of waveguide crossings.
Figure 41: Improvement of multi-layer implementations of Matrix, $\lambda$-router and Snake against the single-layer implementations considering: a) worst-case losses and b) average losses.

A similar trend is observed for the average loss (Figure 41-b). Matrix shows the largest improvement since its single-layer implementation exhibits the highest number of waveguide crossings. For example, for 8x8 Matrix$^{wX}_{ML}$, the two-layer implementation allows to reduce the number of waveguide crossings from 125 to 88.

Figure 42-a and -b detail the loss contribution to the worst-case and average loss respectively for Matrix$^{wX}_{ML}$, Matrix$^{wX}_{ML}$, $\lambda$-router$^{wX}_{ML}$, $\lambda$-router$^{wX}_{ML}$, Snake$^{wX}_{ML}$, Snake$^{wX}_{ML}$, and ORNoC$^{ML}$. A first observation on the worst-case loss evaluation can be made regarding the layouts: for 2x2, 4x4 and 6x6 architecture size, the layout with the shortest waveguide lengths outperforms the layout without any waveguide crossing, independently from the network topology. However, the layout without any waveguide crossing shows better scalability since the loss shows lower sensibility to the architecture size variation. For 8x8 architecture size, it exhibits lower losses for Matrix, $\lambda$-router and Snake. Similar observation can be made for average loss (Figure 42-b).
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Figure 42: a) Worst-case losses and b) average losses evaluation for 2x2 to 8x8 IP cores.

The results indicate that the better scalability would combine the use of: i) multi-layer deposited silicon technology, to reduce waveguide crossings in the network by implementing multiple optical layers; and ii) intra-layer layout that avoids waveguide crossings. ORNoC\textsubscript{ML} gathers these criteria, leading to the lowest worst-case loss despite the long distance introduced by the serpentine layout. For the 8x8 case, the worst-case path in ORNoC\textsubscript{ML} is 1.5dB, lower than Matrix\textsubscript{ML} \textsuperscript{w/oX} with 3.3dB and Matrix\textsubscript{ML} \textsuperscript{wX} with 3.7dB.

By considering the average loss, ORNoC\textsubscript{ML} reduces the average loss by 63% on average compared to the other multi-layer implementations. This significant difference is obtained due to the shorter propagation distance between neighbor IP cores. The improvement reaches 55% and 70% for 2x2 case and 8x8 case, respectively. The average loss is 1.1dB for ORNoC\textsubscript{ML} compared to 2.4dB and 3.2dB for Matrix\textsubscript{ML} \textsuperscript{w/oX} and Matrix\textsubscript{ML} \textsuperscript{wX} under the 8x8 architecture size.

3.5.2.2.2. Distance between the cores

Figure 43-a shows the comparison results for a fixed 6x6 cores with $d$ ranging from 1mm to 3mm, with intervals of 0.5mm. The increase of the loss with the distance is higher for the networks relying on the layout without any waveguide crossing. In all the cases, even for the
longest considered distance (i.e., 3mm, which leads to a 3.24cm² die size), ORNoC\textsubscript{ML} is the most power-efficient network and is followed by Matrix\textsubscript{wX}\textsuperscript{ML} and Matrix\textsubscript{w/oX}\textsuperscript{ML}. Similar trend is observed for the average loss in Figure 43-b.

![Figure 43: Crossbar comparison for 6x6 cores according to a) worst-case losses and b) average losses with distance between cores ranging from 1mm to 3mm.](image)

For the 8x8 size, the implementation of Matrix requires 63 wavelengths with regard to 64 wavelengths for Snake and λ-router. Architectures which include higher number of wavelengths are penalized by the crosstalk and fabrication variability. A more reasonable implementation would be to consider several smaller networks, which implies additional waveguide crossings [16]. The use of the ring topology intrinsically leverages this issue since the number of waveguides can be set according to the crosstalk and process variability requirements. This can be achieved without any waveguide crossing, because of the multi-layer implementation and the use of on-chip laser sources.

Following the methodology from [6], ORNoC\textsubscript{ML} would require 16 waveguides if we consider the optimistic maximum number of 64 wavelengths per waveguides, and 63 waveguides if we
consider more realistic scenario with 16 wavelengths per waveguide. When parallel waveguides are added for Matrix, $\lambda$-router or Snake, additional waveguide crossings are introduced \[16\], even when multi-layer technology is employed. For the ORNoC$\text{ML}$, no additional waveguide crossing is included. This characteristic together with the regularity of its layout turns ORNoC$\text{ML}$ into a scalable structure which does not require any custom place-and-route tool \[5\][17].

### 3.5.2.2.3. Laser output power saving

The minimum laser output power depends on the total loss experienced by the optical signals from the source ONI to the destination ONI. The higher the losses, the higher the required laser output power, i.e., the lower the energy efficiency. It is worth noticing that the received optical power should be high enough to reach the SNR requirements for a given target BER, which is out of the scope of the chapter but has been investigated in Chapter 4. Reducing the losses is thus mandatory to improve the overall system energy efficiency. Among the sources of losses, the most significant ones are those related to the signal propagation in the waveguides, the waveguide crossing and the MR drop. In this section, we investigate the achievable laser output power saving using multi-layer silicon deposited technology.

![Figure 44: Laser output power saving for ORNoC$\text{ML}$ over Matrix$^{\lambda\text{X}}_{\text{ML}}$.](image)

The minimum laser output power required for the communication is evaluated for the two most energy-efficient architectures, i.e., ORNoC$\text{ML}$ and Matrix$^{\lambda\text{X}}_{\text{ML}}$. The laser output power saving ratio for ORNoC$\text{ML}$ over Matrix$^{\lambda\text{X}}_{\text{ML}}$ is shown in Figure 44. For instance, for 2x2 architecture and 2.5mm between the cores, the required laser output power for ORNoC$\text{ML}$ is reduced by 14% compared to the solution with Matrix$^{\lambda\text{X}}_{\text{ML}}$. Results show that power saving under a given architecture size remains similar. However, significant saving is achieved for larger architectures: for a 2.5mm distance, the laser power saving increases from 15% (2x2) to 37% (8x8). The
improvement is due to increasing number of waveguide crossings with Matrix\(^{wX}_{ML}\). It is worth noticing that, these results being provided for the average losses in the communications path, additional power saving could be achieved for ORNoC\(_{ML}\) if tunable lasers output power are used.

3.5.2.3. Crossbar comparisons under technological parameters exploration

Comparisons achieved in the previous sections are based on a given set of losses values. Such analysis may lead to incomplete and/or unfair comparisons. For instance, by considering low propagation losses and high waveguide crossing losses values, layouts without any waveguide crossing will be favored over the layout with the shortest waveguide length. For this purpose, we further compare ORNoC\(_{ML}\) and Matrix\(^{wX}_{ML}\) (i.e., the best networks based on the previous analysis) by exploring technology related parameters. The following results are given for the worst-case loss evaluation under 8x8 architecture sizes.

3.5.2.3.1. Exploration through propagation loss and OVC loss parameters

For the first comparison, \(P_{propagation,1}\) and \(P_{propagation,2}\) are ranged from 0 to 3dB/cm and from 0 to 1.5dB/cm, respectively. Figure 45 show the worst-case loss for Matrix\(^{wX}_{ML}\) (blue color) and ORNoC\(_{ML}\) (green color) assuming 1mm, 1.5mm, 2mm and 2.5mm distances between IP cores. For instance, for \(d=1\)mm (Figure 45-a), \(P_{propagation,1}=0.5\)dB/cm and \(P_{propagation,2}=0.1\)dB/cm, worst-case losses for ORNoC\(_{ML}\) and Matrix\(^{wX}_{ML}\) are 1.0dB and 3.0dB respectively. The worst-case loss for Matrix\(^{wX}_{ML}\) increases linearly with the propagation loss. The trend is different for ORNoC\(_{ML}\) for which communications are allocated on the path showing lower losses: for \(P_{propagation,2}\) smaller than \(P_{propagation,1}\), layer 2 is utilized in priority.

For \(d=1\)mm, ORNoC\(_{ML}\) outperforms Matrix\(^{wX}_{ML}\) for most propagations losses values, including those extracted from [9] and [11]. However, Matrix\(^{wX}_{ML}\) shows lower losses than ORNoC\(_{ML}\) (4.7dB and 5.3dB respectively) around \(P_{propagation,1}=P_{propagation,2}=1.5\)dB values. Obviously, worst-case losses for both Matrix\(^{wX}_{ML}\) and ORNoC\(_{ML}\) tend to increase with larger distance between IPs, which is due to the increased waveguides length. However, the serpentine layout of the ring topology is more impacted by the increased lengths and Matrix\(^{wX}_{ML}\) becomes more efficient than ORNoC\(_{ML}\). However, this trend is limited to region for which the ratio between the propagation losses on the layers remains small. This is further investigated in the following.
Figure 45: Exploration of Matrix\textsuperscript{wX} (in blue) and ORNoC\textsubscript{ML} (in green) worst-case loss according to propagation loss parameters for 8x8 IP cores and four distances: a) d=1mm, b) d=1.5mm, c) d=2mm and d) d=2.5mm. Results are given for $P_{OVC}=0.1\text{dB}$, $P_{\text{drop},i}=0.5\text{dB}$, and $P_{\text{crossing}}=0.05\text{dB}$.

The intersection lines from Figure 45 (i.e., when worst-case losses of Matrix\textsuperscript{wX} and ORNoC\textsubscript{ML} are the same) are reported in Figure 46-a. In the figure, each line corresponds to a distance (i.e., d=1mm, 1.5mm, 2mm, and 2.5mm). The left-hand side of a line is the area for which ORNoC\textsubscript{ML} is more energy efficient than Matrix\textsuperscript{wX}. For Huang [11] propagation loss parameters, Matrix\textsuperscript{wX} is more energy efficient than ORNoC\textsubscript{ML} for d=2mm and d=2.5mm while, for much lower losses parameters from Biberman [9], ORNoC\textsubscript{ML} dominates over Matrix\textsuperscript{wX} for all the distances.

The comparison for 6x6 architecture is illustrated in Figure 46-b. While the trend is similar to the one obtained for 8x8, ORNoC\textsubscript{ML} is more energy efficient than Matrix\textsuperscript{wX} for most design options. As a result, for Huang [11] values, ORNoC\textsubscript{ML} is the most energy efficient solution, independently from the distance. The intersection line for d=1mm is out of the studied propagation loss ranges. This trend is compatible with the observation made in Section 3.5.2.2 and can be summarized as follow: the shift from 8x8 to 6x6 architecture size leads to i) a
reduction in the waveguide crossing for Matrix_{ML}^{wX} and ii) reduced waveguide length for ORNoC_{ML}. The design of ORNoC_{ML} being optimized according to the propagation losses, significant improvements are obtained compared to a naïve allocation of the communication. However, the energy improvement compared to a network with waveguide crossings depends on the crossing losses, which is investigated in the following.

![Figure 46](image)

**Figure 46: Energy efficiency comparison of Matrix_{ML}^{wX} and ORNoC_{ML} according to the propagation loss in layer 1 and layer 2 for a) 8x8 and b) 6x6 cores. The lines represent the values for which Matrix_{ML}^{wX} and ORNoC_{ML} show the same worst-case loss for d=1mm, 1.5mm, 2mm and 2.5mm. For each distance, ORNoC_{ML} is more energy efficient on the left-hand side of the line. Results are given for 8x8 IP cores, \(P_{\text{drop},1}=0.5\text{dB}, P_{\text{crossing}}=0.05\text{dB}, P_{\text{OVC}}=0.1\text{dB}.\)**

### 3.5.2.3.2. Comparison through propagation loss and crossing losses parameters

In the following, we further investigate the comparison between the two interconnects by exploring the crossing loss (i.e., \(P_{\text{crossing}}\) in the 0-0.2dB range [10]) and the propagation loss ratio among the layers (i.e., \(P_{\text{propagation},1}/P_{\text{propagation},2}\)). \(P_{\text{propagation},2}\) is set to 1.3dB/cm [11] and we assume lower losses in layer 2 than in layer 1. Figure 47 illustrates the results for 8x8 cores. We use the same representation as in Figure 46. The area on the right of the line corresponds to design space for which ORNoC_{ML} is more energy efficient than Matrix_{ML}^{wX}. The results help to understand the impact of the crossing and the propagation losses on the network energy efficiencies. For instance, for \(d=2.5\text{mm}\) and 0.15dB crossing loss, ORNoC_{ML} is more energy efficient than Matrix_{ML}^{wX} from a 1.6 propagation ratio. However, if the crossing loss can be reduced to 0.05dB without modification of the propagation loss ratio, then Matrix_{ML}^{wX} is the best network and ORNoC_{ML} should be used only if a 2.8 ratio can be reached.
Chapter 3 Passive topology and layout guidelines

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Figure 47: Energy efficiency comparison of Matrix\textsuperscript{wX} and ORNoC\textsubscript{ML}, according to the crossing loss and the propagation loss ratio. The lines represent the values for which Matrix\textsuperscript{wX} and ORNoC\textsubscript{ML} show the same worst-case loss for d=1mm, 1.5mm, 2mm and 2.5mm. For each distance, ORNoC\textsubscript{ML} is more energy efficient on the right-hand side of the line. Results are given for 8x8 IP cores, P\textsubscript{OVC}=0.2dB, P\textsubscript{drop,1}=0.5dB, P\textsubscript{propagation,2}=1.3dB/cm.

3.5.2.4. Summary of the main results and discussion

The results have shown that multi-layer deposited silicon technology contributes to improve the energy efficiency of optical crossbars thanks to drastic losses reduction. The most significant loss reductions have been observed for layouts that minimize the waveguide length while still allowing waveguide crossings (e.g., Matrix\textsuperscript{wX}, \lambda-router\textsuperscript{wX} and Snake\textsuperscript{wX}). Furthermore, the bigger the architecture, the more the energy saving, e.g., 70% worst-case loss reduction is reached for Matrix\textsuperscript{wX} interconnecting 8x8 cores.

We compared all the multi-layer implementations and by aggregating the contribution of the propagation loss, OVC loss, drop loss and crossing loss in the worst-case loss. Overall, ORNoC\textsubscript{ML} provides the lowest worst-case loss for 2x2 to 8x8 architectures, overcoming the multi-layer implementations of Matrix, \lambda-router and Snake. The higher energy efficiency of ORNoC\textsubscript{ML} is due to i) the serpentine layout (that avoids waveguide crossings) and ii) the design method (that allows allocating communication on optical path showing the lowest losses). For instance, ORNoC\textsubscript{ML} achieves on average 55% and 60% reduction of worst-case and average losses, compared to Matrix\textsuperscript{wX}. For larger architecture size, e.g., 10x10, Matrix, Snake and \lambda-router will reach a physical limitation related to the maximum number of wavelengths per waveguide (e.g., 64 wavelengths [18]). A solution to overcome this limitation is to replicate the network implementation, which leads to additional waveguide crossings and less regular layout.
Using additional optical layers (not only two as in this study) could also help to overcome this issue.

We also investigate the energy efficiency comparison of Matrix$_{ML}$ and ORNoC$_{ML}$ under technological parameters exploration. The results can be used in two ways: first, from a set of technological parameters, it is possible to identify the best topology; second, by targeting a given topology, constraints on technological parameters can be identified.

3.6. Conclusion

Optical crossbars on chip represent an efficient interconnect solution for many-core architectures. In this chapter, single-layer and multi-layer implementations of various crossbars have been proposed, and their worst-case and average losses are evaluated according to topological, layout and technological aspects.

We first compare possible single-layer crossbar implementations relying on Matrix, multistage and ring-based network topologies. For Matrix, $\lambda$-router and Snake topologies, we proposed layouts i) with minimized waveguide length and ii) without waveguide crossing. For a given number of IP cores and a given die size, ring-based networks facilitate the implementation characterized by lower worst-case optical losses, leading to the most power-efficient solution. For the explored design space, ring-based topology implementations exhibit higher power efficiency compared to matrix-based and multistage-based network implementations.

In addition, we have investigated the impact of multi-layer deposited silicon technology on the energy efficiency of corresponding multi-layer crossbar implementations. For the ring topology, a design method has been proposed; it allows allocating communications on optical paths exhibiting the lowest losses. For Matrix, $\lambda$-router and Snake topologies, we also proposed the multi-layer layouts i) with minimized waveguide length and ii) without waveguide crossing. Results show that, to interconnect 8x8 cores, multi-layer implementations lead to on average 42% and 46% reduction in the worst-case and averages losses, respectively. This has an immediate impact on the laser output power, which can decrease up to 85%, thus contributing to a higher energy efficiency of the optical network. The ring is the most energy-efficient topology among all studied architectures: on average, it leads to 66% reduction of worst-case loss when compared to the related topologies. We also investigated the impact of technological parameters
values on the energy efficiency of ORNoC and Matrix. This allows selecting the topology to be used for a given technological platform. The approach of power loss analysis was applied to passive and fully interconnected networks, but it can be extended to active networks requiring resource allocation mechanism. Beyond the multi-layer technology applied in Section 3.3, other technologies could be considered to explore in order to further reduce the optical loss, for example, the optimized optical refractive index in the implementations. In addition, in our future work, we will further investigate the impact of multi-layer silicon deposited on the network thermal sensitivity and robustness to fabrication process variation.

3.7. References


Chapter 4. Thermal-aware design methodology to maximize energy efficiency

Silicon photonic devices are highly sensitive to temperature variation induced by thermal effect over the chip, which leads to a drift of the laser wavelength and MRs resonant wavelength along one communication path. Consequently, the Signal to Noise Ratio (SNR) of the signals received by the photodetector decreases, which leads to a higher Bit Error Ratio (BER) and lower energy efficiency (due to the re-transmission). This is further accentuated by the significant reduction of on-chip lasers efficiency as the temperature increases.

In this chapter, the influence of thermal variation in silicon photonic interconnect is first detailed in Section 4.1. Then, the proposed design methodology is illustrated in Section 4.2 and a thermal-aware on-chip laser tuning method is proposed based on the methodology to maximize the tuning energy efficiency while taking into consideration of BER requirement. In Section 4.3, the models used to evaluate the proposed method are presented. The evaluation results and conclusion are given in Section 4.4 and Section 4.5, respectively.

4.1. Influence of the thermal variation in silicon photonic interconnect

We assume a similar 3D architecture to Chapter 3, i.e., one optical layer on top of one electrical layer. The ONIs are composed of on-chip lasers and MRs, responsible for modulating and receiving the optical signal on the optical layer.

On-chip lasers (e.g., VCSEL-based lasers [8][23]) provide the optical power through current driving. While the fabrication processes of CMOS-compatible VCSEL is less mature than those of microdisk lasers [24], they offer significant advantage in terms of scalability (higher laser output power is achievable and layout can be more flexible) and spectral density due to their small 3dB bandwidth (typically 0.1nm). The drawback of on-chip lasers over off-chip counterpart is their intrinsically lower efficiency and higher sensitivity to the chip activity variation since they are located above the processing layer. More precisely, each on-chip laser is located above a CMOS driver that controls the laser current ($I_{\text{laser}}$), as illustrated in Figure 48-a. The current propagates through a TSV and directly drives the on-chip laser. An optical signal is vertically emitted and is redirected to a horizontal waveguide through a taper. The optical power
injected into the network (\(\text{OP}_{\text{net}}\)) thus depends on i) the intensity of the laser current \(I_{\text{laser}}\), ii) the laser efficiency (\(\eta_{\text{laser}}\)) and iii) the taper coupling efficiency (\(\eta_{\text{coupling}}\), assumed to be 80%). For instance, the VCSEL efficiency is highly sensitive to its temperature: it can drop from 15% at 40°C to 4% at 60°C. This rather low efficiency leads to a high dissipated power (\(P_{\text{laser}}\)) which, together with the power dissipated by the CMOS driver (\(P_{\text{driver}}\)) and the chip part at source area/surrounding (\(P_{\text{chip}}\)), influences the on-chip laser temperature. Hence, for a given driven current, the power of the emitted optical signal (\(\text{OP}_{\text{laser}}\)) depends on the laser temperature, which is influenced by \(P_{\text{chip}}\), \(P_{\text{laser}}\) and \(P_{\text{driver}}\), as illustrated in Figure 48-a. The influence of laser temperature on signal propagation is shown in Figure 48-b.

Figure 48: a) Generic communication in silicon photonic interconnects, considering the thermal effect. The efficiency of an on-chip laser (e.g., VCSEL) and the emitted signal wavelength depend on its temperature, which is influenced by the CMOS driver and the chip activity. The MR resonant wavelength depends on the MR temperature, which is influenced by the lasers, chip activity and MR tuning power. b) The signal at modulation (mark “\(\Phi\)” represents the electrical data before modulation, and mark “\(\Phi\)” represents the optical signal after modulation); c) The signal at photodetection (mark “\(\Phi\)” represents the optical signal before photodetection, and mark “\(\Phi\)” represents the electrical data after photodetection).

In the meanwhile, the emitted signal wavelength is influenced by the laser temperature. Ideally, the laser wavelength is designed to be equal with the corresponding MR resonant wavelength at the target side, as well as the MRs along the path. However, the MR resonant
wavelength can also drift with its temperature. For instance, the temperature of the MR at photodetector is influenced by the power dissipated by the chip part at the target area/surrounding ($P'_{\text{chip}}$) and also the on-chip laser ($P'_{\text{laser}}$) (Figure 48-a). In short, the signal power dropped by the MR at the target side ($OP_{\text{pd}}$) also depends on the wavelength alignment among the optical devices, influenced by the gradient temperature among different interfaces, as illustrated in Figure 48-c. Thus, a low average temperature and gradient temperature is necessary.

Furthermore, for an increasing activity of the processing layer (which is expected to result in additional communications), either the optical interconnect bandwidth will decrease assuming a same laser current (i.e., the BER being higher, data will be re-emitted) or the optical interconnect power consumption will increase (i.e., a higher laser current is required to compensate the reduced efficiency). The laser current thus must be carefully selected since i) a too small value will lead to high BER and ii) a too high value will lead to a power hungry solution.

To conclude, silicon-based optical devices are sensitive to thermal variation (0.1nm/°C typically [4]), which induces the mismatch of the wavelengths of silicon photonic devices along one communication channel. As a result, the optical signal power received at the reader side decreases, which results in a lower SNR and a higher BER. In addition, the efficiency of on-chip lasers is reduced when the temperature increases, i.e., the BER is further degraded. In order to deal with this issue, we propose a thermal-aware design methodology to ensure a targeted BER at the reader side while minimizing the power consumption.

4.2. Proposed Methodology

In this section, we present a proposed methodology allowing to design a thermal-robust silicon photonic interconnect.

4.2.1. Methodology overview

The proposed methodology (in Figure 49) aims to achieve a compromise between energy efficiency and reliability, and allows the exploration of design space at both device level and system level. For this purpose, the main characteristics of the optical devices (e.g., lasers, MRs, waveguides, photodetectors) are taken into account in device-level models. Architectural aspects such as interconnect size, topology/layout, and implementation technologies are taken into account at the system-level models, as shown in “IP Models” of Figure 49.
Figure 49: Proposed thermal-aware design methodology with a combination of system level and device level.

Key input parameters at device level (e.g., laser driver current ($I_{laser}$) and MR tuning power ($P_{MR}$)) and system level (e.g., chip activity and communication scheme) are specified by users. $I_{laser}$ and $P_{MR}$ can be tuned to align wavelengths of laser and MRs. Different chip activities (e.g., uniform, diagonal, and corner) simulate the power dissipated by the processing layer and communication scheme determines signal paths.

Based on a set of device-level and system-level input parameters, thermal simulation performs thermal analysis. It allows the estimation of temperature profiles over the chip, providing gradient temperature and average temperature of optical components. In our methodology, thermal sensitivity of on-chip laser sources is taken into account. From the generated temperature maps, established analytical models (i.e., power model and BER model) allow the evaluation of energy efficiency and reliability of the considered optical interconnects,
Chapter 4 Thermal-aware design methodology to maximize energy efficiency

with tuning power consumption and BER as metrics. The results from the power analysis and BER analysis are the basis of design space exploration and optimization.

For a given system-level input parameter, tuning device-level input parameters (i.e., $I_{\text{laser}}$ and $P_{\text{MR}}$) allows design space to be explored at both device-level and system-level, as shown by the red arrow in Figure 49. In the meanwhile, this allows a compromise to be achieved between energy efficiency and reliability of the optical interconnects. In addition, this methodology is generic and can be applied to both stationary and transient analysis. In case that the device-level and system-level models are changed, the flow of the methodology still works, just in need of updating the models.

Based on the methodology, we propose a thermal-aware on-chip laser tuning method to overcome the wavelength variation induced by temperature variation, while achieving the targeted BER in the meanwhile. The novelty of the method relies on the tuning of the laser driver current, which ideally complements traditional methods such as MRs tuning and channel remapping [2][3]. While the method is evaluated for on-chip laser sources, it is also suitable for off-chip lasers since the impact of a temperature elevation would remain the same.

4.2.2. Signals and MRs wavelengths alignment

Figure 50: a) MWSR channel with one wavelength and two writers, b) transmission without thermal variation (ideal case), c) transmission considering MR tuning only method with off-chip laser sources, and d) transmission with our proposed on-chip laser tuning method.
Figure 50 illustrates our method in the context of a MWSR channel [1] with a single laser source, 2 writers and one reader. In our work, we consider distributed lasers that are located in the same layer with MRs, waveguide and photodetectors. For this purpose, we assume the use of CMOS-compatible laser sources such as VCSELs, for which the size is similar to the one of MRs. As illustrated in Figure 50-a, ONI_m communicates with ONI_r: the MR in the intermediate ONI_i is turned OFF while the MR in ONI_m is in the modulation state (state OFF and ON to modulate data ‘1’ and ‘0’ respectively).

Figure 50-b illustrates the ideal transmission of a data ‘1’ that occurs when there is no temperature variation along the communication path. The optical signal injected by the laser (which is characterized by a power OP_{ideal} and a wavelength \( \lambda_{\text{laser}} \)) crosses ONI_m and ONI_i, propagates along the waveguide until ONI_r where it is dropped to the photodetector (as illustrated by the blue transmission lines in the Figure 50-b). The power of the optical signal decreases along the path due to the waveguide propagation losses and the MRs crossing losses (blue line in Figure 50-b). The BER is estimated based on the received optical power OP_{pd,ideal}, the receiver sensitivity and the crosstalk (induced by other transmitting signals at different wavelengths, not illustrated here for the sake of clarity but taken into account in our models).

### 4.2.2.1. Existing MR tuning only method

In case of temperature gradient over the communication path, the resonant wavelength of the MRs will drift (see the red transmission lines in Figure 50-c) while the wavelength of the emitted signal (\( \lambda_{\text{laser}} \)) remains the same in case off-chip lasers are considered. Without compensating the effect of this drift, the misalignment between the signal wavelength and the MRs resonant wavelengths leads to significantly increased BER. To overcome this effect, the MRs along the waveguide are tuned back to their initial positions (the grey transmission lines in Figure 50-c) using thermal tuning or voltage tuning. The post-tuning signal transmission is illustrated by the blue line in Figure 50-c: the received optical power is slightly lower than in the ideal scenario due to marginal wavelengths misalignment. The MRs tuning power depends on their temperature drift (\( \Delta T_{\text{MR},m} \), \( \Delta T_{\text{MR},i} \) and \( \Delta T_{\text{MR},r} \)) and the thermal sensitivity coefficient \( \rho_{\text{MR}} \). The total power consumption of the channel is given by the sum of the laser power consumption \( P_{\text{laser}} \) and the MRs tuning power \( \sum P_{\text{MR}} \).
4.2.2.2. Proposed laser and MR tuning method

The key novelty of our method relies on the laser bias current tuning: since the laser temperature varies with its bias current, the wavelength of the optical signal can be tuned. Hence, in addition to tuning the MRs to align the resonant wavelengths with the optical signal, we also tune the wavelength of the optical signal itself, which contributes to reduce the power required to compensate the thermal variation.

As illustrated in Figure 50-d, tuning the driver current $I_{\text{las}}$ has an impact on the laser power consumption and the emitted signal wavelength: the former varies from $P_{\text{laser}}$ to $P'_{\text{laser}}$ and the latter shifts from $\lambda_{\text{laser}}$ to $\lambda'_{\text{laser}}$. Therefore, under the same temperature gradient considered in Figure 50-c, the MRs wavelengths need to be tuned to $\lambda'_{\text{laser}}$, instead of $\lambda_{\text{laser}}$ (see the green transmission lines in Figure 50-d). The MRs tuning power decreases since the wavelengths distance is reduced. As a drawback, the power of the emitted signal is reduced, meaning that a tradeoff needs to be defined in order to reach the target BER while decreasing the total power consumption of the channel. It is worth noticing that, although the method is illustrated with a 1-wavelength channel, it is generic and it can be applied to WDM channels, as illustrated in the results section. Moreover, it is complementary to related methods providing channel remapping [2][3] that we have adapted to minimize the tuning power instead of the tuning distance.

4.3. Models

This section presents the models used for BER and tuning power estimations, i.e., transmission model, power model, and simulation model.

Figure 51: Generic MWSR channel.

Figure 51 illustrates a generic MWSR channel with lasers and $N_{\text{ONI}}$ interfaces ($N_{\text{ONI}}$-1 writers and 1 reader). $N_{\text{WL}}$ lasers inject the optical signals into one single waveguide by using a
multiplexer, i.e., \(N_{WL}\) wavelengths can be used for communicating within the MWSR channel. In the figure, the signal modulation occurs in ONI\(_0\) (i.e., the first writer). In the following, we define analytical models to evaluate i) the MWSR channel communication quality through a BER estimation and ii) the tuning power consumption (\(P_{tuning}\)) required to align the wavelengths of the optical signals with the MRs.

### 4.3.1. Transmission model

In Figure 51, the optical signals modulated with data \(d_j\) propagate through the intermediate writers (i.e., ONI\(_i\), \(i=1, \ldots, N_{ONI-2}\)) until reaching the reader, i.e., the targeted \((N_{ONI-1})^{th}\) ONI. The optical power received by the photodetector at \(\lambda_j\) (\(OP_{pd,j,d_j}\)) is composed of i) the expected optical signal at \(\lambda_j\) (\(OP_{signal,j,d_j}\)) and ii) the crosstalk (\(OP_{crosstalk,j,d_j}\)) from the other signals at \(\lambda_k\) (where \(k=0, 1, \ldots, N_{WL}-1\), and \(k\neq j\)). The signal transmission is thus composed by i) the transmission through the writers (\(T_w\)) and ii) the transmission through the reader part (\(T_r\)). Hence, the received optical power is defined as:

\[
OP_{pd,j,d_j} = \sum_{k=0}^{N_{WL}-1} (T_{w,d_j}[k] \cdot T_{r,j}[k] \cdot OP_{laser}[k]) \tag{4.1}
\]

The expected received signal power is:

\[
OP_{signal,j,d_j} = T_{w,d_j}[j] \cdot T_{r,j}[j] \cdot OP_{laser}[j] \tag{4.2}
\]

And the received crosstalk is:

\[
OP_{crosstalk,j,d_j} = \sum_{k=0}^{N_{WL}-1} (T_{w,d_j}[k] \cdot T_{r,j}[k] \cdot OP_{laser}[k]) \ (k\neq j) \tag{4.3}
\]

We consider the signal at wavelength \(\lambda_k\) received by the \(j^{th}\) photodetector as a general case. The transmission in the writers part (\(T_{w,d_j}[k]\)) and the reader part (\(T_{r,j}[k]\)) are detailed as following equations.

\[
T_{w,d_j}[k] = (L_\theta)^{N_{wl}[k]} (L_p)^{f_{w,wrl}[k]} (\prod_{n=0}^{N_{wl}-1} \phi_l(\lambda_k, \lambda_n + \Delta \lambda))^N_{wl} \cdot (\prod_{n=0}^{N_{wl}-1} \phi_l(\lambda_k, \lambda_n + d_n \cdot \Delta \lambda)) \tag{4.4}
\]

\[
T_{r,j}[k] = (L_\theta)^{N_{wl}[k]} (L_p)^{f_{w,wrl}[k]} \prod_{n=0}^{f_{r}-1} \phi_r(\lambda_k, \lambda_n) \phi_d(\lambda_k, \lambda_j) \tag{4.5}
\]
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Here, \( \phi_t \) and \( \phi_d \) are the signal transmission on MR through port and drop port (detailed in Section 4.3.1.1). \( L_b \) and \( L_p \) are the bending loss and the propagation loss, which are assumed to be 0dB and 0.5dB/cm in this work. \( l_{w,{\text{total}}}[k] \) and \( l_{r,{\text{total}}}[k] \) (resp. \( N_{w,b}[k] \) and \( N_{r,b}[k] \)) are the total waveguide length (resp. number of waveguide bends) experienced by signal at \( \lambda_k \) in writers and reader parts. \( \Delta \lambda \) is the MR wavelength shift between ON and OFF states.

On the reader side, the receiver sensitivity gives the minimum optical signal power that can be detected by a photodetector. For a given receiver sensitivity, the SNR can be calculated as follow.

\[
\text{SNR} = \frac{R \cdot (OP_{pd,j,1} - OP_{pd,j,0})}{i_n} \tag{4.6}
\]

where \( i_n \) is the photodetector internal noise (4\( \mu \)A [7] in this work), \( R \) is the responsivity of the photodetector (1A/W in this work). \( OP_{pd,j,1} \) and \( OP_{pd,j,0} \) is the optical power received for the modulation of data “1” and “0” respectively. The worst-case SNR is estimated by considering

\[
OP_{pd,j,1} = OP_{signal,j,1} \tag{4.7}
\]

\[
OP_{pd,j,0} = OP_{crosstalk,j,0} \tag{4.8}
\]

The BER is obtained as following:

\[
\text{BER} = \frac{1}{2} \text{erfc}\left(\frac{\text{SNR}}{2\sqrt{2}}\right) \tag{4.9}
\]

4.3.1.1. MR transmission model for signal analysis

The received power depends on the transmission of the optical signals in the through port and the drop port of a MR (Figure 52-a). A MR is characterized by a resonant wavelength (\( \lambda_{\text{res}} \)) in the ON state, i.e., the input signals at \( \lambda_{\text{signal}} = \lambda_{\text{res}} \) are redirected to the drop port. In the OFF state, the resonant wavelength drifts by \( \Delta \lambda \), i.e., the input signals at \( \lambda_{\text{signal}} \neq \lambda_{\text{res}} \) will continue propagating in the same waveguide. Figure 52-b-c illustrates the transmissions on through port and drop port (i.e. \( \phi_t \) and \( \phi_d \)) in ON and OFF states respectively. The actual transmissions depend on the device geometry (i.e. ring radius, \( R \)), the self(cross)-coupling coefficient (i.e. \( r_1, r_2, k_1 \) and \( k_2 \)), the power attenuation coefficient \( \alpha \), and the single-pass phase shift \( \theta(\lambda_{\text{signal}}, \lambda_{\text{res}}) \). Table 7 summarizes the parameters and equations (4.10) and (4.11) give the transmission \( \phi_t \) and \( \phi_d \) extracted from [22].
Figure 52: MR model: a) device geometry, signal transmission on through port and drop port in b) ON state and c) OFF state.

### Table 7: Transmission parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$r_1$, $r_2$</td>
<td>Self-coupling coefficient</td>
<td>µm</td>
</tr>
<tr>
<td>$k_1$, $k_2$</td>
<td>Cross-coupling coefficient</td>
<td>µm</td>
</tr>
<tr>
<td>$R$</td>
<td>MR radius</td>
<td>µm</td>
</tr>
<tr>
<td>$n_{res}$</td>
<td>Effective refractive index of MR (varies with applied voltage, device geometry and ambient temperature)</td>
<td></td>
</tr>
<tr>
<td>$m$</td>
<td>Resonant mode number of MR</td>
<td></td>
</tr>
<tr>
<td>$\lambda_{res}$</td>
<td>MR resonant wavelength</td>
<td>nm</td>
</tr>
<tr>
<td>$\lambda_{signal}$</td>
<td>Signal wavelength</td>
<td>nm</td>
</tr>
<tr>
<td>$\Delta \lambda$</td>
<td>MR wavelength between ON and OFF states</td>
<td>nm</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>Power attenuation coefficient</td>
<td>dB/cm</td>
</tr>
<tr>
<td>$a(\lambda_{res})$</td>
<td>Single-pass amplitude transmission</td>
<td></td>
</tr>
<tr>
<td>$\theta(\lambda_{signal}, \lambda_{res})$</td>
<td>Single-pass phase shift</td>
<td></td>
</tr>
<tr>
<td>$L_b$</td>
<td>180° bending loss under 40µm radius</td>
<td>dB</td>
</tr>
</tbody>
</table>

\[
\varphi_t(\lambda_{signal}, \lambda_{res}) = \frac{a^2(\lambda_{res})r_2^2 - 2a(\lambda_{res})\eta r_2 \cos[\theta(\lambda_{signal}, \lambda_{res})] + r_1^2}{1 - 2a(\lambda_{res})\eta r_2 \cos[\theta(\lambda_{signal}, \lambda_{res})] + [a(\lambda_{res})\eta r_2]^2} \tag{4.10}
\]

\[
\varphi_d(\lambda_{signal}, \lambda_{res}) = \frac{a(\lambda_{res})(1-r_1^2)(1-r_2^2)}{1 - 2a(\lambda_{res})\eta r_2 \cos[\theta(\lambda_{signal}, \lambda_{res})] + [a(\lambda_{res})\eta r_2]^2} \tag{4.11}
\]
4.3.2. Power model

The total tuning power consumption of a MWSR channel is divided into two parts: i) the lasers power consumption \( P_{\text{laser}} \) and ii) the MRs tuning power \( P_{\text{MR}} \) as in equations (4.12), (4.13), and (4.14). Table 8 summarizes the parameters involved in the model and the following details the lasers and MR models we assume.

\[
P_{\text{tuning}} = P_{\text{MR}} + P_{\text{laser}} \tag{4.12}
\]

\[
P_{\text{MR}} = \sum_{i=0}^{N_{\text{ONI}}-1} \sum_{j=0}^{N_{\text{WL}}-1} P_{\text{MR},i,j} \tag{4.13}
\]

\[
P_{\text{laser}} = \sum_{j=0}^{N_{\text{WL}}-1} P_{\text{laser},j} \tag{4.14}
\]

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( N_{\text{ONI}} )</td>
<td>Number of ONIs in the network</td>
<td></td>
</tr>
<tr>
<td>( N_{\text{WL}} )</td>
<td>Number of wavelengths per interface</td>
<td></td>
</tr>
<tr>
<td>( P_{\text{MR},i,j} )</td>
<td>Tuning power of the MR(_j) in ONI(_i)</td>
<td>mW</td>
</tr>
<tr>
<td>( P_{\text{laser},j} )</td>
<td>Power consumption of laser(_j)</td>
<td>mW</td>
</tr>
<tr>
<td>( T_{E,i,j} )</td>
<td>Tuning efficiency (voltage tuning or thermal tuning) of the MR(_j) in ONI(_i)</td>
<td>m</td>
</tr>
<tr>
<td>( \lambda_{\text{laser},j} )</td>
<td>Wavelength of laser corresponding to the wavelength(_j) after tuning</td>
<td>nm</td>
</tr>
<tr>
<td>( \lambda_{\text{MR},i,j} )</td>
<td>Wavelength of MR(_j) in ONI(_i) considering the wavelength drift</td>
<td>nm</td>
</tr>
<tr>
<td>( \lambda_{\text{laser,room}} )</td>
<td>Wavelength of laser, at room temperature</td>
<td>nm</td>
</tr>
<tr>
<td>( \lambda_{\text{MR,room}} )</td>
<td>Wavelength of MR(_j) in ONI(_i) at room temperature</td>
<td>nm</td>
</tr>
<tr>
<td>( \rho_{\text{MR}}, \rho_{\text{laser}} )</td>
<td>Temperature sensitivity factor of MR and laser wavelengths</td>
<td>nm/°C</td>
</tr>
<tr>
<td>( \Delta T_{\text{MR,room}} )</td>
<td>Temperature drift of MR(_j) in ONI(_i) and laser(_j)</td>
<td>°C</td>
</tr>
<tr>
<td>( \Delta T_{\text{laser,room}} )</td>
<td>Temperature of the MR(_j) in ONI(_i) and laser(_j)</td>
<td>°C</td>
</tr>
<tr>
<td>( T_{\text{room}} )</td>
<td>Room temperature as reference</td>
<td>°C</td>
</tr>
<tr>
<td>( FSR )</td>
<td>Free Spectral Range</td>
<td>nm</td>
</tr>
</tbody>
</table>
4.3.2.1. Laser

Figure 53: PCM-VCSEL: a) 3D view extracted from [8] and the cross-section view including the taper, b) wavelength drift of VCSEL ($\Delta\lambda_{\text{laser}}$) according to temperature drift ($\Delta T_{\text{laser}}$) considering temperature sensitivity ($\rho_{\text{laser}}$) as 0.1nm/°C, and c) output power of laser ($OP_{\text{laser}}$) wrt. $T_{\text{laser}}$ and $I_{\text{laser}}$. Curves b) and c) are obtained by extrapolation of data from [8].

In this work, we consider the PCM-VCSELs (illustrated in Figure 53-a) as on-chip laser sources. They rely on a double set of Si/SiO$_2$ photonic crystal mirrors (PCMs). PCM-VCSELs are considered due to their micrometer-scale layer thickness (thinner than VCSELs using DBR), their broadband reflectivity, full control over the cavity modal, and polarization emission features [8]. Moreover, PCM-VCSELs are CMOS compatible. The fabrication employs standard
CMOS pilot line processing tools and high-yield full-wafer bonding of group III-V alloys on silicon [8].

Coupling the vertical light from VCSEL into a horizontal waveguide can be achieved by using a taper located on the layer of the top PCM and the waveguide. We assume an 80% coupling efficiency, which is slightly pessimistic compared to the 85% simulated in [9]. The signal wavelength ($\lambda_{\text{laser}}$) can be tuned by changing the laser temperature ($T_{\text{laser}}$) since the laser is sensitive to the thermal variation (assumed as 0.1 nm/°C [8]), as shown in Figure 53-b. Under a given driver current ($I_{\text{laser}}$), the laser efficiency will decrease with an increase of the temperature ($T_{\text{laser}}$), which leads to a reduction of the emitted optical signal ($OP_{\text{laser}}$), as shown in Figure 53-c. The relationship between the wavelength and the temperature is given as:

$$\lambda_{\text{laser},j} = \lambda_{\text{laser},j,\text{room}} + \Delta \lambda_{\text{laser},j}$$  \hspace{1cm} (4.15)

$$\Delta \lambda_{\text{laser},j} = \rho_{\text{laser}} \cdot \Delta T_{\text{laser},j}$$  \hspace{1cm} (4.16)

$$\Delta T_{\text{laser},j} = T_{\text{laser},j} - T_{\text{room}}$$  \hspace{1cm} (4.17)

Since the lasers are located above the processing layer, their temperature is influenced by i) the driver current ($I_{\text{laser}}$) and ii) the chip activity. The laser power consumption ($P_{\text{laser},j}$ for a laser at $\lambda_j$) can be estimated as:

$$P_{\text{laser},j} = [slop_{\text{ohm}} \times (I_{\text{laser},j} - I_{\text{th}}) + 1] \times I_{\text{laser},j} \times slop_{\text{W/A}} \times (I_{\text{laser},j} - I_{\text{th}})$$  \hspace{1cm} (4.18)

where $slop_{\text{ohm}}$, $slop_{\text{W/A}}$ and $I_{\text{th}}$ are the laser voltage slope, the output power slope and the threshold current, respectively.

### 4.3.2.2. Microring Resonators (MRs)

The modulation is realized by electro-optic effect on the MRs. Forward biased is applied to perform voltage tuning, which leads to a blue shift of the resonant wavelength. MRs can be classified according to their junction, PN or PIN. With a PN junction, the reverse biasing changes the refractive index through carrier depletion while, with a PIN junction, the refractive index is changed by carrier injection. Although PN junctions allow a faster switching time compared to PIN junctions, the higher extinction ratio provided by PIN junction leads to better communications. In this work, we thus consider the use of PIN junctions only.
Since the MRs are sensitive to temperature, their resonant wavelength needs to be tuned to ensure a proper alignment of the signal wavelength $\lambda_{laser,j}$ with the MR wavelength $\lambda_{MR,i,j}$. The MR tuning power ($P_{MR,i,j}$) depends on the distance between the wavelengths. MR tuning can be achieved by using electro-optic and thermo-optic effects [12], as illustrated in Figure 54 (monitor and feedback-control parts are not shown). The following recurs to the tuning methods:

$$P_{MR,i,j} = T E_{i,j} \cdot |\lambda_{laser,j} - \lambda_{MR,i,j}|$$  \hspace{1cm} (4. 19)

$$\lambda_{MR,i,j} = \lambda_{MR,i,j,room} + P_{MR} \cdot \Delta T_{MR,i,j}$$  \hspace{1cm} (4. 20)

$$\Delta T_{MR,i,j} = T_{MR,i,j} - T_{room}$$  \hspace{1cm} (4. 21)

**Voltage Tuning (VT) for blue shift:** Voltage tuning is fast but its range ($VTr$) is limited to 1nm [4]. We denote $VTe$ as the voltage tuning efficiency (typically 0.13mW/nm [6][16]).

**Thermal Tuning (TT) for red shift:** the MR resonant wavelength can be red shifted by using local micro-heater [10]. Thermal tuning is slower than voltage tuning but its operating range ($TTr$) can reach 20nm [21]. The thermal tuning efficiency $TTe$ is lower (typically 0.24mW/nm [6][16]).

4.3.3. **Simulation model**

From the estimation of the tuning power and the BER, we define exploration strategies to i) reduce the power consumption by maintaining a targeted BER and ii) decrease the BER as much
as possible and estimate the power cost. Both methods require tuning the laser bias current and will be further detailed in Section 4.4.3.

To evaluate these methods, the temperature of the optical devices (i.e., on-chip lasers and MRs) along the communication channel and under a given chip activity is needed. For this purpose, *IcTherm*\(^1\) [13] is used to provide thermal maps of the silicon photonic interconnect. *IcTherm* is a thermal simulator for electronic devices which accurately models their complex structure and provides 3D full-chip temperature maps. *IcTherm* solves the physical equations that govern the temperature in the chip, using the Finite Volume Method [14], a numerical method for solving partial differential equations. It was validated against the commercial simulator COMSOL [15]: its maximal error was found to be less than 1% [13].

In order to perform thermal evaluations, our architecture model is based on the real physical structure of the system. The different components of the system (i.e., package, die, heat sources, and optical devices) are represented as rectangular blocks, defined by their dimension, their position, and a constitutive material (e.g., Figure 55). The blocks can be assigned to power values (i.e., \(I_{\text{laser}}\) and \(P_{\text{MR}}\)) as the input of simulation, which allow modeling the heat sources of the system. For instance, in Figure 55, \(I_{\text{laser}}\) is indicated by the power of laser. The Back-End-Of-Line (BEOL) is modeled as a thin layer (10µm) and the heat sources (i.e., cores, cache, router, etc.) are represented as rectangular blocks with power values, situated in the BEOL layer.

\[\text{component}\]
\[\text{name}=\text{laser}\]
\[\text{dimension}=15e-6,37e-6,1.4e-6\]
\[\text{material}=\text{inp+ingaasp}\]
\[\text{position}=2.5e-6,6e-6,1.4e-6\]
\[\text{power}=4e-3\]

**Figure 55:** Instance of optical component model, e.g., laser.

The structure of the system is discretized into small cubic cells that match the distribution of the materials and the heat sources. Figure 56 illustrates the discretization of a section of the system. Because the interfaces contain micro-scale components (e.g. TSVs, VCSELs and CMOS drivers), we use a fine-grain resolution with a cell size of 5 µm × 5 µm for meshing the region.

\(^1\) *IcTherm* website: http://www.ictherm.com/
containing the interfaces. For the rest of the system, we use a coarser resolution with a cell size of \(100 \mu m \times 100 \mu m\) for the heat sources and \(500 \mu m \times 500 \mu m\) for the package.

![Diagram of cell and materials](image)

**Figure 56:** IcTherm computes the heat transfers between the cells and outputs the temperature value of each cell. This thermal map allows computing the gradient temperature between any points of the system.

### 4.4. Results

This section describes the system we consider and then evaluates the efficiency of the proposed method.

#### 4.4.1. Case study

##### 4.4.1.1. Targeted system

![Diagram of packaging and layers](image)

**Figure 57:** Packaging of the SCC chip and the optical interconnect.
Figure 57 shows the global view of the targeted system, which contains the following components: steel back-plate, motherboard, socket, Intel’s Single-Chip Cloud Computer (SCC chip) with silicon-photonic interconnects and on-chip laser sources, copper lid and heat sink.

The considered 3D architecture is based on SCC (Figure 58-a) with a stacked optical layer. Figure 58-b shows the abstract layout of SCC we use for the considered architecture layout. The silicon photonic interconnect is placed on top of the SCC chip and thermal simulations are performed using IcTherm [13]. The Section 4.4.1.2 details the optical interconnect we considered for the results.

4.4.1.2. Optical communications based on WDM

To evaluate the proposed method, we consider the MWSR-like architecture (in Figure 59) as an instance of the optical interconnect, with on-chip lasers such as PCM-VCSELs utilizing NWL wavelengths ($\lambda_0, \lambda_1, \ldots, \lambda_{NWL-1}$). The light vertically emitted by the laser is coupled into a waveguide by using a taper (not shown in the figure for the sake of clarity). Multiple laser wavelengths are combined together into a single waveguide with a multiplexer (“MUX” for short in Figure 59), which can be implemented by a multimode interference (MMI) coupler [5]. The wavelengths are equally distributed in order to reduce the crosstalk.

The optical signal (supplied by on-chip lasers) is modulated by one of the writers and propagates to the reader for detection and conversion. An interface is composed of i) writers for modulating signal and ii) one reader for detecting and receiving signal. The writer is composed of NWL MRs. The reader uses passive MRs and photodetectors to filter and detect the expected signal respectively.
In the architecture example illustrated in Figure 59, we assume 4 interfaces, meaning that there are 4 MWSR channels. In this example, we also assume a single waveguide per channel. There are thus 3 writers and 1 reader per channel, each writer being composed of $N_{WL}$ modulators and the reader being composed of $N_{WL}$ photodetector/passive MR couples.

4.4.2. **Temperature maps under different chip activities and laser power consumption**

![Temperature maps](image)

Figure 60: Considered interconnect layouts including 4, 6, 8 and 12 interfaces with a-d) on-chip lasers and e-h) off-chip lasers.
We assume 4 architectures including 4, 6, 8 and 12 interfaces, as illustrated in Figure 60. The number of interfaces gives the number of MWSR channels. In the figure, a single waveguide per channel is represented and only parts of the channels are illustrated for the 12 interfaces architecture for the sake of clarity. For comparison purpose, we assume architectures with on-chip lasers (Figure 60 a-d) and off-chip lasers (Figure 60 e-h). On-chip lasers are placed out of the interface in order to limit the temperature variation of the MRs as the laser driver current is tuned. The off-chip lasers are placed all around the chip in order to reduce the additional-insertion losses (i.e., from waveguide propagation and waveguide crossing).

<table>
<thead>
<tr>
<th>chip activity</th>
<th>( P_{\text{laser}} )</th>
<th>4mW</th>
<th>8mW</th>
<th>12mW</th>
</tr>
</thead>
<tbody>
<tr>
<td>uniform 10%</td>
<td>10% 10%</td>
<td><img src="image1.png" alt="Image" /></td>
<td><img src="image2.png" alt="Image" /></td>
<td><img src="image3.png" alt="Image" /></td>
</tr>
<tr>
<td></td>
<td>10% 10%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>diagonal 25%-50%</td>
<td>25% 50%</td>
<td><img src="image4.png" alt="Image" /></td>
<td><img src="image5.png" alt="Image" /></td>
<td><img src="image6.png" alt="Image" /></td>
</tr>
<tr>
<td></td>
<td>50% 25%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>corner 50%-5%</td>
<td>50% 5%</td>
<td><img src="image7.png" alt="Image" /></td>
<td><img src="image8.png" alt="Image" /></td>
<td><img src="image9.png" alt="Image" /></td>
</tr>
<tr>
<td></td>
<td>5% 5%</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure 61**: 2D temperature maps of the photonic layer for various chip activities (i.e., uniform 10%, diagonal 25%-50% and corner 50%-5%) and laser power consumption (i.e., 4mW, 8mW, and 12mW).

Figure 61 illustrates photonic layer temperature maps for the layout given in Figure 60-a, assuming 4 waveguides per MWSR channel and 16 wavelengths per waveguide (i.e., there is a total of 64 laser sources per channel). DDR3 memory controllers and PLL have been shut down to highlight the impact of chip activity and laser power consumption on the temperature. In order to illustrate the variety of application to be executed, we consider three values for the laser power consumption (i.e., 4mW, 8mW, and 12mW) and three chip activities (i.e., uniform 10%, diagonal 25%-50% and corner 50%-5%). For instance, the corner activity is assumed for the case where the communication occurs through the memory controller on the top-left side. This figure
highlights the important thermal gradient in the lasers region. It is worth noticing that, by considering the VCSELs described in Figure 53, only very limited lasing effect is obtained for temperature above 80°C. Such scenario occurs for a 50% local activity and 12mW laser power consumption (see the red hotspot region). The impact of the chip activity and the laser power consumption on the BER will be investigated in the following.

From the resulting thermal map, the proposed laser tuning method is applied in order to i) evaluate the BER using the transmission models and ii) evaluate the total channel power consumption \( P_{\text{tuning}} \) (including the laser power consumption \( P_{\text{laser}} \) and the MR tuning power \( P_{\text{MR}} \)).

### 4.4.3. Impact of the laser bias current on the BER and the power consumption

We evaluate our method for a 12 interfaces architecture (i.e., 12 MWSR channels with 11 writers and 1 reader per channel), 1 waveguide and 4 wavelengths (i.e., 4 lasers per waveguide and 4 MRs per writer). The study focuses on a single MWSR channel. We run thermal simulations under uniform 15% and 20% chip activity (i.e., 18.75W and 25W, respectively), with the tuning current \( I_{\text{laser}} \) ranging from 0mA to 16mA. Figure 62 represents the laser temperature drift \( \Delta T_{\text{laser}} \) and the optical output power \( O_{\text{P_{laser}}} \) deduced from the resulting thermal maps. It is worth noticing that, compared to Figure 53-c, a much higher sensitivity to the driver current is obtained due to the locally dissipated energy, which contributes to the temperature elevation. Indeed, Figure 53-c corresponds to characterization results obtained under a temperature stabilized using a Peltier cooling system. In Figure 62, the laser response is simulated in a 3D integrated circuit without cooling system.

![Figure 62: Impact of \( I_{\text{laser}} \) on the optical output power \( O_{\text{P_{laser}}} \) and the laser temperature drift \( \Delta T_{\text{laser}} \) under uniform 15% and 20% chip activities.](image)
For $I_{\text{laser}}=0.05\text{mA}$ under uniform 15% chip activity, $\Delta T_{\text{laser}} = 26^\circ\text{C}$ and there is no lasing effect (i.e. $\text{OP}_{\text{laser}}=0\text{mW}$) since the lasing current threshold for the corresponding temperature is not reached. Lasing effect starts at $I_{\text{laser}}=1\text{mA}$ and a maximum of 0.65mW optical power is obtained for 8mA. For this current value, the laser drift temperature is 36.8°C. Above 8mA, the laser efficiency drastically decreases due to the temperature elevation. From the laser only point of view, the most relevant $I_{\text{laser}}$ current values ranges from 1mA to 8mA. However, from the whole MWSR channel point of view, current values above 8mA can also be relevant since a drift of the signal wavelengths accompanies the laser temperature elevation. Depending on the context, this may allow the reduction of the power needed to tune the MRs on the MWSR channel. For 20% chip activity, a similar trend is observed but $\Delta T_{\text{laser}}$ is slightly higher, which in turns leads to a reduction of the outputted light.

### 4.4.3.1. Results for uniform chip activities

From the thermal maps over the optical layer, with a laser power consumption $P_{\text{laser}}$ ranging from 1mW to 22mW (obtained by tuning the laser injection current $I_{\text{laser}}$), we evaluate the total power required to align the MRs resonant wavelengths with the emitted signals. We also evaluate the worst-case BER among all the channels in the network, as illustrated in Figure 63. For 25% chip activity (in red), for small laser injection current (i.e., $P_{\text{laser}}$ ranging from 1mW to 5mW), the optical power of the emitted signal is too low to compensate the channel losses, which results in a high BER. Then, the communication quality improves as the laser injection current increases: the BER reaches its optimal value at $P_{\text{laser}}=9\text{mW}$. By considering a static design method, the corresponding injection current will be selected to ensure the best communication quality. Above 9mW, the laser efficiency decreases due to the increase of the local temperature, leading to a higher BER. The channel power consumption is also given in the figure. It is composed of the laser power consumption (simply reported from the x-axis) and the MRs tuning power.

Figure 63 gives the tuning power consumption and the BER under 25% chip activity (in red). When the chip activity drops to 20% (in blue), two methods can be followed:

- To achieve a given BER (e.g., $10^{-12}$), the laser current can be reduced to minimize the tuning power, as represented by $a\rightarrow b$ arrow in Figure 63. In this example, the tuning power drops from 8.7mW to 7.4mW, i.e., 15% reduction.
- To minimize the BER, the laser current is slightly increased, as illustrated by $c \rightarrow d$ arrow in Figure 63. In this example, the tuning power increases from 12.8mW to 14.2mW (i.e., 11% power cost). However, the BER remains optimal and decreases from $10^{-17}$ to $10^{-27}$ (for 25% and 20% chip activity respectively).

As reflected in the thermal maps, the gradient temperature within each interface remains below 1°C. The total tuning power of each MWSR channel can thus be obtained.

Simulations results show that the targeted $10^{-12}$ BER couldn’t be reached for chip activity higher than 30%, independently from the selected laser power consumption. This limitation is directly related to the thermal sensitivity of the laser, for which the efficiency drops for temperature above 40°C. The laser efficiency is further explored in Section 4.4.4.

![Figure 63: Tuning power ($P_{\text{tuning}}$) and BER for a MWSR channel with 12 interfaces, 4 wavelengths per waveguide under 20% and 25% uniform chip activities. FSR=59nm, $m=17$, voltage tuning efficiency $V_T=0.13\text{mW/nm}$, thermal tuning efficiency $T_T=0.24\text{mW/nm}$ [6][16].](image)

### 4.4.3.2. Results for diagonal chip activities

We also run thermal simulations for 10%-30% and 30%-10% diagonal chip activities. Figure 64 gives the results for the MWSR channel with laser sources located on the top-left hand side of the chip (i.e., blue channel in Figure 60-d). 4mW and 5mW laser power consumption allow the total power consumption (while still achieving $10^{-12}$ BER) to be minimized for 10%-30% and 30%-10% activities, respectively. As expected, the maximum reachable BER is better for 10%-30% activity due to the lower heat locally dissipated by the chip (i.e., the optical signals outputted by the lasers is higher). An interesting trend is the slightly lower MRs tuning for 10%-30% activity, which is due to a reduced distance between the MRs resonant wavelengths and the
laser wavelengths. While this power saving only slightly influences the total channel energy figures, significant gains are reachable for larger chip activity gradient, which is evaluated in the following.

Figure 64: $P_{\text{tuning}}$ and BER under 10%-30% and 30%-10% diagonal activities. Interconnect and technologies assumptions are those used in Figure 63.

4.4.3.3. Results for corner chip activities

Figure 65 illustrates the total tuning power and the BER under a) 20%-70%, b) 20%-75% and c) 20%-85% corner activities. In this scenario, we only consider the MWSR channel with laser sources located in the 20% chip activity region since an insufficient lasing effect is obtained for lasers located in the region with higher activity.

In Figure 65-a, for $P_{\text{laser}}=1\text{mW}$, 33.6mW are required to align the MRs resonant wavelengths with the, significantly distant, optical signals. Increasing $P_{\text{laser}}$ to 2mW leads to a reduction of the wavelengths distance, which in turn helps reducing $P_{\text{MR}}$ to 23.3mW. $P_{\text{MR}}$ continues shrinking until wavelengths are aligned, which is obtained for $P_{\text{laser}}=5\text{mW}$ (mark a in the figure). This value is 1mW more than the minimum $P_{\text{laser}}$ allowing the targeted $10^{-12}$ BER to be reached. The optimal BER is obtained for $P_{\text{laser}}=10\text{mW}$ (mark b). In Figure 65-b, the targeted BER is obtained starting from $P_{\text{laser}}=5\text{mW}$. However, for this value, the wavelengths distance to compensate is still significant and leads to $P_{\text{MR}}=7.4\text{mW}$. By increasing $P_{\text{laser}}$ to 7mW (mark c), 6.5mW can be saved on the MRs tuning, which leads to a more power efficient solution. This corresponds to the scenario sketched in Figure 50. Due to a slightly higher temperature, the optimal BER is obtained for $P_{\text{laser}}=10\text{mW}$ (mark d). The same trend can be observed in Figure 65-c: $P_{\text{laser}}=6\text{mW}$
allows the BER requirements to be reached but $P_{\text{laser}}=9\text{mW}$ is a globally more power efficient solution. Furthermore, $P_{\text{laser}}=9\text{mW}$ also leads to the optimal BER (mark $e$), thus demonstrating the potential for adaptive laser tuning methods to maximize the energy efficiency of nanophotonic interconnects.

**Figure 65:** $P_{\text{tuning}}$ and BER under a) 20%-70%, b) 20%-75% and c) 20%-85% corner chip activities. Interconnect and technologies assumptions are those used in Figure 63.

Finally, a slight 5% increase of the corner gradient activity (i.e., 20%-90%, not shown in the figure) will avoid reaching the targeted BER for $P_{\text{laser}}=12\text{mW}$, while $P_{\text{laser}}=9\text{mW}$ still achieves it.
This demonstrates that for the considered system, an adaptive method relying on laser tuning not only reduces the energy, but also helps covering a wider range of chip activities.

4.4.4. Laser efficiency comparison

In this section, we consider two laser efficiencies and we evaluate their impact on the tuning power. Figure 66-a represents a conservative and an aggressive scenario. The conservative scenario corresponds to the laser already detailed in Figure 53 and the aggressive one is obtained by considering a \( \times 2 \) laser efficiency. The tuning power is illustrated in Figure 66-b for uniform chip activities ranging from 5\% to 25\%, where we assume 12 interfaces. The targeted BER is set to \( 10^{-12} \), which requires less energy with aggressive scenario since the receiver optical power is higher for a same bias current.

\[
\begin{align*}
\text{Conservative} & \quad \text{Aggressive} \\
\text{Temperature (℃)} & \quad \text{Temperature (℃)} \\
0 & \quad 0 \\
10 & \quad 10 \\
20 & \quad 20 \\
30 & \quad 30 \\
40 & \quad 40 \\
50 & \quad 50 \\
60 & \quad 60 \\
70 & \quad 70
\end{align*}
\]

![Figure 66: a) Laser efficiency for conservative and aggressive scenarios and b) \( P_{\text{tuning}} \) for 5\%, 10\%, 15\%, 20\% and 25\% chip activities. Interconnect and technologies assumptions are those used in Figure 63.](image)

Hence, for a 5\% chip activity, \( P_{\text{tuning}} \) is reduced from 5.0mW (conservative) to 3.6mW (aggressive). The improvement of the laser efficiency leads to an increase of the ratio of the MR tuning in the channel total power consumption. For instance, for 5\% chip activity, the MR tuning power ratio increases from 40\% to 45\%. However, due to the higher efficiency of the laser, tuning the laser becomes more efficient than tuning the MRs, which leads to a reduction of the MRs tuning power (i.e., 2.0mW and 1.6mW for conservative and aggressive scenario...
respectively). The combined reduction of laser tuning and MRs tuning leads to significant global energy saving, e.g., 28% for 5% chip activity. Further power saving are obtained for higher chip activities (e.g., 47% under 25% chip activity). These results would help investigating laser requirements for ultra-low power silicon photonics interconnects.

4.4.5. **Tuning methods comparison**

We compare our method with related solutions in which only MR tuning is used. We consider related solutions relying on off-chip and on-chip lasers. For off-chip lasers, the laser wavelength is fixed and the resonant wavelengths of the MRs along a given channel may need to be tuned back to be aligned with the laser, considering channel remapping. We also take into account waveguide crossing losses (considered as 0.05dB per crossing), assuming a single waveguide is used per channel. We assume the same characteristics for off-chip and on-chip lasers and a 80% coupling efficiency has been considered, which is slightly optimistic compared to the 74% demonstrated in [17]. For on-chip lasers with MR tuning only method, we take into account the wavelength drift of the emitted optical signal due to the temperature variation to evaluate the energy needed to tune the MRs. With our method, the laser bias current $I_{\text{laser}}$ is tuned.

![Figure 67: Channel energy efficiency w/ and w/o laser tuning for 12 interfaces. FSR=59nm, m=17, $V_{\text{Tt}}=0.13\,\text{mW/nm}$, $T_{\text{Tt}}=0.24\,\text{mW/nm}$ [6][16].](image)

We consider a 12 interfaces architecture with 4 to 16 wavelengths per MWSR channel and a 10Gb/s data rate. The initial chip activity is assumed to be 15% and the laser power consumption is set to achieve a given BER (e.g., $10^{-12}$). Figure 67 illustrates the contributions of the laser and the MR tuning power (without considering the modulation) for 4 to 16 wavelengths. Our method is the most power efficient for all the studied cases. For instance, for 4 wavelengths MWSR
channels, we reach 2.0pJ/bit wrt. 2.5pJ/bit and 16.4pJ/bit for related on-chip and off-chip methods respectively. When the number of wavelength increases, additional energy is needed since the number of MRs considerably increases.

The results show that, for 16 wavelengths, the optical channels using off-chip lasers give comparable power results to our method. It is also worth noticing that the results obtained for the off-chip lasers method are optimistic for 3 reasons. First, we assume off-chip lasers working at a constant 25°C room temperature, which requires an energy consuming cooling system not taken into account here. Second, we assume a single waveguide per MWSR channel, which leads to at least 11 waveguide crossing for a 12 interfaces architecture illustrated in Figure 60-h (e.g., it leads to 0.55dB losses on each waveguide). MWSR channels with more than 4 waveguides are regularly considered in the literature, which would significantly increase the losses. Third, the propagation loss due to the longer waveguides has not been considered. However, additional scenarios, including application dependent chip activities, should be considered to further consolidate this comparison.

![Figure 68: Design tradeoff between BER and energy efficiency for 12 interfaces.](image)

To further compare our method with the MR tuning only method, we also evaluate for which number of wavelengths the BER is the best. For this purpose, we lower as much as possible the BER when the chip activity decreases from 25% to 20% and we evaluate the required energy. We assume 12 interfaces and a number of wavelengths ranging from 4 to 16. As shown in Figure 68, the energy/bit remains slightly constant with the number of wavelengths (approx. 1.2 pJ/bit). However, the BER significantly increases from $10^{-27}$ (4 wavelengths) to $10^{-12}$ (16 wavelengths), i.e., the communication quality is better for small number of wavelengths. Such method allows the maintaining of a given BER level to satisfy applications constrained by communication
quality. Overall, these results show that the MWSR channels with a small number of wavelengths provide a better BER. This leads us to conclude that our method tends to be the most power efficient for this range of wavelengths.

4.4.6. **Energy saving under a given BER**

We evaluate the potential gain of the proposed laser tuning method with the traditional on-chip laser (for which only MRs tuning is possible). For this purpose, we first set the laser power consumption to 9mW in order to reach a targeted $10^{-12}$ BER for the highest considered chip activity (25% in this example). We then reduce the chip activity to 20%, 15% and 10%, and we evaluate the achievable power reduction while still reaching $10^{-12}$ BER [18][19]. As illustrated in Table 9, up to 52% reduction is obtained for a 10% chip activity. In case a $10^{-9}$ BER [20][21] turns to be acceptable (i.e., in order to match the requirements of an application to be executed), the energy consumption can be further decreased. These results demonstrate the significant energy reductions achievable by using chip activity-aware methods.

<table>
<thead>
<tr>
<th>Chip activity</th>
<th>Target BER</th>
<th>20%</th>
<th>15%</th>
<th>10%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Target BER</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$10^{-12}$</td>
<td></td>
<td>42%</td>
<td>52%</td>
<td>52%</td>
</tr>
<tr>
<td>$10^{-9}$</td>
<td></td>
<td>53%</td>
<td>53%</td>
<td>63%</td>
</tr>
</tbody>
</table>

We evaluate the energy saving of our method for various numbers of interfaces and wavelengths and by assuming the same technique as previously described. As shown in Figure 69:

**Figure 69: Energy saving for our joint laser and MR tuning method wrt. MR tuning only method for different channel configurations.**
Chapter 4 Thermal-aware design methodology to maximize energy efficiency

69, the energy saving is the smallest for 12 interfaces and 16 wavelengths but it still reaches 46% wrt. the MRs tuning only method. On average, 63% energy saving is obtained.

4.5. Conclusion

Thermal variation has a negative impact on the communication reliability and energy efficiency. Based on our analysis of the influence of the thermal variation, we propose a methodology to design thermal-robust silicon photonic interconnect, optimizing energy efficiency while meeting the reliability requirement at the same time.

The methodology allows exploration of the design space at both device level and system level. For this purpose, the main characteristics of the optical devices are taken into account in device-level models. Architectural aspects are taken into account at the system-level models. Input parameters at device level and system level can be specified by users. Based on a set of device-level and system-level input parameters, analyses (i.e., thermal analysis, power analysis and BER analysis) are performed to evaluate the energy efficiency and reliability. In details, thermal simulation performs thermal analysis and allows estimating temperature profiles over the chip. From the generated temperature maps, established analytical models (i.e., power model and BER model) estimate the tuning power consumption and BER. Design space exploration can then be carried out, by tuning device-level input parameters under a given system-level input parameter. In the meanwhile, this allows a compromise to be achieved between energy efficiency and reliability of the optical interconnects.

Based on the methodology, we propose to jointly tune lasers and MRs to improve the energy efficiency of fully integrated nanophotonic interconnects. For this purpose, we have defined a method relying on thermal simulations and crosstalk analyses, taking into account the thermal sensitivity of the laser sources. Evaluations have been carried out for a 3D stacked architecture interconnecting processors with MWSR-like optical channels. We have assumed CMOS compatible PCM-VCSELs for the light sources and the layout of the optical layer has been designed to avoid waveguide crossing. Design space exploration covered the number of interfaces, the number of wavelengths and the laser efficiency, taking into account uniform, diagonal and corner chip activities.

Compared to methods for which laser tuning is not possible, results show that a combined tuning of laser and MRs leads to 63% energy reduction when the uniform chip activity decreases
from 25% to 5%. BER-energy tradeoffs have been explored and allow strategies to be defined to minimize either the energy, or the BER. As a key result, we have shown that, under specific chip activities, increasing the laser power consumption allows both energy and BER to be improved. This trend has been observed for a MWSR channel interconnecting 12 interfaces. We also showed that, by being able to tune the laser power within the 6-12mW ranges, the targeted $10^{-12}$ BER is reachable in all the scenarios we covered, assuming a maximum 25% chip activity in the region where the lasers are located. This strong limitation directly depends on the laser efficiency, which drastically decreases above 40°C. Major technological improvements are thus needed to make silicon photonics become a realistic and viable solution for on-chip interconnects in fully integrated 3D architectures. While such improvement would lead to more energy efficient optical channels by reducing the laser power consumption, it is worth noticing that our joint laser and MRs tuning method would further contribute to this objective by also reducing the MRs tuning power.

### 4.6 References


Chapter 4 Thermal-aware design methodology to maximize energy efficiency

Chapter 5. CHAMELEON: CHANNEL Efficient Optical Network-on-Chip

In Chapter 3, we explored several topologies and found that the ring topology exhibits higher energy efficiency by taking into consideration the worst-case loss. In addition, combining clockwise (C) and counter-clockwise (CC) communication directions is able to further reduce the worst-case loss and then enhance the energy efficiency. To make good use of these good properties, a solution is considered in the point view of architecture.

In this chapter, we propose CHAMELEON, which stands for CHANNEL Efficient ONoc, a reconfigurable channel efficient optical network on chip (ONoC). The reconfiguration of CHAMELEON can be specified at design-time by using static mapping method, or achieved at run-time through a communication protocol. Compared with existing ONoCs, the main features of the proposed architecture are summarized as following: Firstly, CHAMELEON extends the SWSR approach (i.e., ORNoC, previously described in chapter 3) with a reconfigurability feature, allowing opening and closing dedicated channels between IP cores. Hence, the network bandwidth is highly adaptable according to the communication requirements. Secondly, the same wavelength can be utilized on non-overlapping waveguide parts, thus leading to a highly utilized network and higher bandwidth by considering waveguide partitioning. Thirdly, through the combined use of on-chip lasers and both clockwise and counter-clockwise directions for signal propagation, power consumption can be reduced. Finally, higher scalability and easy layout synthesis are obtained due to regular ONIs and ring topology.

The chapter is organized as following. In Section 5.1, the proposed architecture and its reconfigurability are introduced. In Section 5.2, the configuration method at design time is presented first. Then the configuration method at run time is detailed in Section 5.3. The loss model used to evaluate the networks is introduced in Section 5.4 and the results are shown in Section 5.5. At last, the discussion and conclusion are given in Section 5.6 and 5.7, respectively.

5.1. Reconfigurability in CHAMELEON

CHAMELEON is implemented in an optical layer, on top of an electrical layer implementing IP cores, similar to the 3D architecture presented in Chapter 3. The topology and layout are
serpentine-like, similar to ORNoC [1]. CHAMELEON also allows the reuse of wavelengths to realize several independent communications in a single waveguide by considering waveguide partitioning.

5.1.1. Interface architecture

One main advantage and difference of CHAMELEON is reconfigurability, compared to ORNoC. This property is primarily enabled by its ONI. Similar to ORNoC [1] (presented in Chapter 3), each ONI consists of a receiver part and a transmitter part crossed by a waveguide, implementing the operations of injection, pass through and ejection on the signal. However, the main distinctions of interfaces can be summarized into two points. Firstly, the interfaces in CHAMELEON are active and able to configure as required bandwidth, while the ones in ORNoC are passive and static as designed. In this sense, CHAMELEON shows more flexibility in bandwidth distribution. Secondly, the interfaces of CHAMELEON are homogeneous and the available wavelengths in receiver part are identical to those in transmitter part, while the ones of ORNoC are heterogeneous and specific to communications. That is to say, the interfaces in CHAMELEON are regular, facilitating the network scalability and layout synthesis.

In details, to implement WDM with N wavelengths in CHAMELEON, N MRs and N on-chip lasers in the same set of specific wavelengths are used in the receiver part and transmitter part, respectively. Each MR can be turned ON or turned OFF, in order to respectively carry out ejection (receive) or pass through operations on the signals at the corresponding wavelength.

Figure 70: Optical Network Interface.
Similarly, each on-chip laser can also be turned ON or turned OFF (in the case of unused state), so as to separately realize injection (send) or pass through operations of the signals. When no communication occurs, all the MRs and laser sources are turned OFF for energy saving. They are turned ON/OFF according to the configuration specified by the electrical control network (formed by the electrical parts of ONIs), in order to allocate resources dynamically according to the communication to be realized. In brief, the reconfigurability relies on the independent control of each MR/laser source, enabled by the electrical control network.

In Figure 70, for instance, optical signal propagating along the waveguide will cross the MRs in the receiver part. If signal wavelength (e.g., $\lambda_0$ or $\lambda_1$, in red and green respectively) matches with that of MR in ON state, it will be dropped into the perpendicular waveguide (i.e., ejection operation), and reach the corresponding photodetector to convert back into electrical form. Otherwise, the signal propagates along the waveguide without being ejected and no optical signal at the same wavelength is injected for the sake of coherency and to avoid interference. Thus, the signal crosses the ONI without any operation, as represented by the signal at wavelength $\lambda_2$ (in blue color) in Figure 70, meaning that the receiver for this signal is in another ONI further along the waveguide.

In the transmitter part, the electrical data coming from the IP cores are converted into current, used to control an on-chip laser. For this purpose, the laser would be turned ON. The optical signal (e.g., $\lambda_1$ in green) is emitted and injected into the waveguide, and then propagates until reaching the receiver part of the destination ONI. It is important to notice that the ejected wavelengths (i.e., $\lambda_0$ and $\lambda_1$) in the receiver part can be reused for the remaining part further along the waveguide. For example, the wavelength $\lambda_1$ in the transmitter part of the ONI is reused to realize another communication. Since each laser is wavelength-specific, the selection of this wavelength to realize a communication relies on the assignment which may be determined at design time or run time. These two reconfiguration methods in CHAMELEON are detailed in the following sections: i) application mapping at design time (in Section 5.2), and ii) communication protocol at run time (in Section 5.3).

5.1.2. Communication schemes

CHAMELEON is able to realize multiple communication schemes due to the reconfigurability, as illustrated in Figure 71.
Figure 71: Possible communication schemes: a) SWSR, b) SWMR, c) MWSR, and d) high-bandwidth channel.

- **SWSR** (Single Writer Single Reader, i.e., dedicated point-to-point communication channels), is facilitated by waveguide partitioning, which allows a given wavelength to be reused in order to realize multiple independent communications in the same waveguide. In Figure 71-a, $\lambda_0$ is used to realize communications ONIA$\rightarrow$ONIB, ONIB$\rightarrow$ONIC and ONIC$\rightarrow$ONIA. Concurrently, $\lambda_1$ and $\lambda_2$ are used to realize ONIC$\rightarrow$ONIB and ONIA$\rightarrow$ONID respectively. This facilitates the virtual partitioning of a waveguide for a given wavelength.

- **SWMR** (Single Writer Multiple Readers, i.e., broadcast/multicast) can be realized by opening dedicated communication channels between a source ONI and all the remaining ONIs (resp. the destination ONIs). In Figure 71-b, ONIB broadcasts data to ONIC, ONID and ONIA through wavelengths $\lambda_0$, $\lambda_1$ and $\lambda_2$ respectively.

- **MWSR** (Multiple Writers Single Reader) can be performed by opening communication channels between several source ONIs and one identified destination ONI. In Figure 71-c, ONIA, ONIB, and ONIC respectively send data at $\lambda_0$, $\lambda_1$ and $\lambda_2$ to the destination interface ONID.
In addition, high-bandwidth channels can be opened by allocating multiple wavelengths for a given communication. This is suitable for the execution of streaming applications that require the transfer of a large amount of data from one IP core to another. In Figure 71-d, high-bandwidth communication channels are opened from ONIB to ONID and from ONID to ONIA.

These communication schemes can be combined as long as sufficient bandwidth in the network is available. For instance, high band width channels can be opened, while other lower bandwidth channels are already open. This high flexibility makes CHAMELEON suitable to execute applications in various classes. However, opening channels at the granularity of the wavelength leads to a higher complexity in the control network, which may result in additional latency during the allocation of optical resources to channels. To make CHAMELEON efficient, each channel should thus transmit as large set of data as possible before its closing. This suits the streaming model of computation particularly well, since it usually requires the transfer of large amount of data during a short period. Moreover, since CHAMELEON allows different channels to be combined within a single configuration at the same time, a high flexibility/reusability degree is reached.

![Figure 72: Bi-directional communication channels. Blue and red colors represent C and CC directions, respectively.](image)

The communication schemes in Figure 71 are illustrated by using one waveguide, meaning only one communication direction is available, for instance, clockwise (C) in the figure. In fact, multiple waveguides can be used to propagate optical signals in both clockwise (C) and counter-
clockwise (CC) directions, as illustrated in Figure 72. In addition to reducing the worst-case losses in the network (consequently the power consumption, as will be discussed later on), this allows bi-directional dedicated communication channels to be opened, which will be suitable for processor–memory communications. The combined use of WDM and multiple waveguides also leads to a high overall bandwidth in the optical network.

5.2. Application mapping at design time

CHAMELEON can be configured at design time: implementing communications specific to the mapping of a streaming application. The configurations generated by this method lead to networks characterized by low latency (i.e., no arbitration is required) and high energy efficiency (i.e., dedicated channels are used).

Reconfiguring CHAMELEON leads to setup of a given connectivity between IP cores that can well suit the targeted application to be executed (e.g., streaming) or the architectures

---

**Figure 73:** Configuring CHAMELEON according to communication requirements: a) task mapping on the architecture, b) configured communication channels, c) detailed configuration of ONI B and G, and d) bandwidth matrix.
communication requirements (e.g., processor to memory). The more wavelengths and waveguides there are, the higher the bandwidth is, i.e., the performance improvement with regard to electrical interconnects. However, this comes at the cost of resource overhead and eventually performance penalty, meaning that design tradeoffs need to be explored. This exploration is driven by application cases, which is introduced in the following example mapping of a streaming application onto the targeted architecture. In the example, we consider 8 IP cores connected through 8 ONIs (i.e., A, B, …, H) with a single waveguide. We also assume that 6 wavelengths are available (i.e., $\lambda_0, \lambda_1, \ldots, \lambda_5$).

Figure 73-a represents a MP3 audio decoder application inspired from [2]. This simple application is chosen only to illustrate the approach; it is obvious that optic will be advantageous only for applications requiring huge data transfer. The application is represented as a Directed Acyclic Graph $G = (T, E)$, where $T$ is a set of tasks (i.e., $t_i$) and $E$ a set of data (i.e., $e_{ij}$ to be transferred from task $i$ to task $j$). The right-hand side of Figure 73-a represents the 8 ONIs crossed by the waveguide propagating optical signals. The arrows (“application” -> “architecture”) represent the mapping of the 17 tasks onto the IP cores connected to the ONIs, considering the constraint that source and sink are mapped onto a same IP core. Such mapping solution can be obtained from methods similar to [3] and adapted to silicon photonic interconnect properties. Figure 73-b represents the configured communication channels using a representation highlighting the use of the 6 wavelengths. Wavelengths are allocated according to the inter-ONI communications implied by the mapping (i.e., the intra-ONI communications such as $t_1 \rightarrow t_3$ are realized locally by the corresponding IP core). For instance, the data dependencies $t_0 \rightarrow t_1$ and $t_0 \rightarrow t_2$ in the application lead to the configuration of channels between A and B (e.g., with $\lambda_0$, $\lambda_1$ and $\lambda_2$), and between A and C (e.g., with $\lambda_3$, $\lambda_4$ and $\lambda_5$) respectively (i.e., a multicast is realized). In this example, 3 wavelengths are allocated to each channel, i.e., the bandwidth is equitably shared. Depending on the data dependencies between the tasks (as specified in the application model), the wavelengths can be shared diversely. For instance, between G and H, 5 wavelengths and 1 wavelength are allocated to the channel implementing $t_{11} \rightarrow t_{13}$ and $t_{14} \rightarrow t_{16}$, separately. The resulting configuration leads to a contention-free execution of the application. Figure 73-c represents the configuration of MRs and lasers in ONI B and G and Figure 73-d gives the resulting connectivity/bandwidth matrix.
5.3. Communication protocol at run time

CHAMELEON can be reconfigured at run time, due to the fact that MRs and lasers are reconfigurable. The configuration process is managed by a control network implemented on the electrical layer and is triggered when IP core to IP core communications occur. The control network allows optical resources in the optical network to be reserved, in order to configure dedicated channels between a source IP and a destination IP. Channels are reconfigured at run time by a communication protocol detailed as following.

5.3.1. Protocol overview

A protocol allows communication bandwidth to be allocated between a source and a destination IP. The bandwidth allocation is obtained by configuring ONIs to open dedicated communication channels from a source ONI to a destination ONI (while crossing intermediate ONIs). This is accomplished by allocating one or several wavelengths on the partitions of the waveguide between the source and the destination. The allocation process is initiated by a source IP through the injection of a reservation message RES in the control network. The message will propagate through the intermediate ONIs until reaching the destination ONI. During the propagation of the message, free MRs and lasers (corresponding to free wavelengths) are reserved in the intermediate ONIs for the realization of the dedicated communication channels. We assume that a particular wavelength will be assigned to (or associated with) one communication. Once the message reaches the destination, an ACK message is sent back to the source IP, propagating in the opposite direction and managing to allocate reserved resources for the corresponding source to destination IP. Reserved resources may also be freed if the required bandwidth is reached (the required bandwidth is given by the number of requested wavelengths in the RES message). Once the ACK message is received by the source IP, the laser sources corresponding to the allocated wavelength are turned ON and the modulated optical signal is injected into the optical network. The optical signals go through the intermediate ONIs and are dropped to the photodetectors of the ONI connected to the destination IP. Once the source IP finishes sending the data, a release message is injected into the control network in order to free the allocated resources.

NACK messages allow the reservation process to be cancelled if no bandwidth is available. Then the reservation message must be re-emitted later on by the source IP. RELEASE messages
allow reserved resources to be freed while the reservation message propagates along the network in case that a reserved wavelength is not available along the whole communication path.

<table>
<thead>
<tr>
<th>M_TYPE</th>
<th>M_ID</th>
<th>S_ID</th>
<th>D_ID</th>
<th>Req_WL_NUM</th>
<th>WL_0</th>
<th>WL_1</th>
<th>...</th>
<th>WL_M</th>
</tr>
</thead>
</table>

Figure 74: Control message.

Figure 74 illustrates the structure of control messages. It contains information of the message type (i.e., RES, ACK, NACK and RELEASE), the message ID (M_ID), the ID of the source IP (S_ID), the ID of the destination IP (D_ID), the requested number of wavelengths (Req_WL_NUM) and the states of the requested wavelengths (WL_0, WL_1, …, WL_M). Regarding Req_WL_NUM, the more wavelengths are requested, the higher is the bandwidth between a source and a destination, which thus impacts the transmission time of the data injected into the optical network. The state of the requested wavelengths indicates whether a wavelength is Requested (R) or Not-Requested (NR) to realize the corresponding communication.

5.3.2. Resource allocation algorithm

The configuration of communication channels relies on resource allocation algorithms processing control messages transmitted through the control network. When a control message is emitted, the requested number of wavelength is determined. All the lasers corresponding to the available wavelengths in the transmitter part of the ONI are reserved and the state of the corresponding wavelengths in the message is set to Requested (R). While the control message is propagating in the control network, ONIs might update the state of wavelengths to Not-Requested (NR) if the wavelengths and the corresponding laser sources are not available. Figure 75 illustrates the algorithm step by step. In this example, IP_A initiates a communication with IP_C, which leads to the transmission of messages between ONI_A and ONI_C to open the communication channel (e.g., Req_WL_NUM is set to 1, meaning that one wavelength is requested). We also assume that ONI_C receives data from another ONI through λ_1 (i.e., the green signal in Figure 75) and ONI_B sends data to another ONI through λ_0 (i.e., the red signal in Figure 75). In order to initiate the communication from ONI_A and ONI_C, all the wavelengths available in ONI_A are reserved in order to evaluate whether they are available along the path to ONI_C. Since λ_1 is already used for another communication, lasers specific to λ_0 and λ_2 are reserved (mark ⊙) and RES message is emitted accordingly (mark ⊙).
Figure 75: Example of communication channel opening: a) RES message is emitted, b) RES and REL messages are propagated and generated respectively, c) ACK message is generated and d) data are transmitted through the optical dedicated channel (e.g., \( \lambda_2 \) is used).

For each RES message received by ONI, the destination ID in the control message is first compared to its own ID in order to identify whether the message reaches the destination. If an intermediate ONI is reached, the following algorithm is executed:

**Algorithm to manage RES message in intermediate ONIs**

1. if none of requested WL is Free
2. if at least one requested WL is Used
3. wait until a requested WL becomes Free
4. Else
5. wait for a threshold time
6. if none of the request resource is Free or Used //possible deadlock
7. generate NACK message
8. end execution of the algorithm
9. End if;
10. End if;
11. End if;
12. Set the corresponding MR and laser resources to Reserved
13. If not all the requested resources can be Reserved
14. Update the message content // WL not granted are set to NR
15. Generated REL message and transmit backward
16. End if;
17. Propagate RES message to the next ONI

In this algorithm, the state of each requested wavelength in the message is compared to the local state of the corresponding MR and the laser in the receiver and transmitter part (line 1),
respectively. Possible states of MR and laser are: 1) “Free” (F) meaning that the resource is not involved in the realization of any channel in the optical network; 2) “Used” (U) meaning that the resource is involved in a communication channel; 3) “Reserved” (R) meaning that the resource is reserved by a prior RES message attempting to realize another communication channel. If available, the state of the corresponding MR and laser source is changed from F to R (line 12, mark ③ in Figure 75). In the message itself, the state of each requested wavelength, for which the resource is not free, is changed to NR (line 14, corresponding to “U” state of MR). A REL message is sent backward to the source (line 15, mark ⑤) in order to free the already reserved resources, once the corresponding resources in an ONI are not available. Since the MR and laser source for \( \lambda_0 \) are not available in ONI_B, the state of the reserved MR and laser for \( \lambda_0 \) in ONI_A are updated from R to F (mark ⑥). If at least one requested wavelength can be reserved in the intermediate ONI (i.e., to implement the through operation), the message is forwarded to the next ONI (line 17, mark ⑦). In case none of the requested wavelength can be reserved because resources are already involved in a communication channel, the message is queued locally, waiting for resources to be released and allowing to process the reservation (line 3). Deadlock might occur in all the requested resources that are already reserved (line 6). This scenario might lead to a situation where control messages are reserving resources without being able to reach the destination. In order to prevent deadlock, a counter is started and, if it times out, the reservation process is cancelled and a NACK message is transmitted backward to the source, freeing all the reserved resources (line 7). The source thus re-emits the reservation message after a random latency.

In the case where the reservation message reaches the destination ONI, the only resource that needs to be reserve is MR, since the objective is to terminate the reservation of communication channel. Therefore, the state of the corresponding MRs in the destination ONI is changed to “U” and they are turned ON, thus realizing the drop mode (mark ⑦). Then, an ACK message is sent backward to the source to validate the allocation of the optical resources and to configure the dedicated communication channel (mark ⑧): based on the allocated wavelengths, the status of previously reserved resources in intermediate ONIs is set to free (R→F) (i.e., similarly to the release message) or to used (R→U) (i.e., indicate the reserved resources). Once the ACK message arrives at the source, the reserved laser is set to U, that is to say, is turned ON (injection mode), and the data are transmitted through the optical network (mark ⑧). The requested number
of wavelength (Req_WL_NUM) is also considered as following: if the requested MRs are free, the corresponding set of wavelengths is used to meet the bandwidth requirement. Otherwise, smaller total number of wavelengths is used, thus providing lower bandwidth than the requested.

5.4. Adapted optical loss model

Similar to the model in Chapter 3, the minimum laser output power \( (OP_{\text{min\_laser}}) \) required for a given BER can be obtained by considering the worst-case loss, as shown in equation (5.1).

\[
OP_{\text{dB\_mini\_laser}} = L_{\text{WC}}^{\text{dB}} + OP_{\text{sensitivity}}^{\text{dB}}
\]  

Here, \( OP_{\text{min\_laser}} \) (in dBm), \( L_{\text{WC}} \) (in dB), and \( OP_{\text{sensitivity}} \) (in dBm) represent the minimum laser output power, the worst-case loss along the optical paths, and the minimum received optical power for a given BER (i.e., receiver sensitivity).

Regarding the losses, bending loss is assumed to be negligible as in Chapter 3. By adapting the general loss model in Chapter 3, the total loss along one optical path \( L_{\text{total}} \) depends on the propagation loss in the waveguide \( L_{\text{propagation}} \) (in dB), the through loss \( L_{\text{through}} \) (in dB) and \( L_{\text{drop}} \) (in dB). Thus, the loss model is simplified as following:

\[
L_{\text{total}}^{\text{dB}} = L_{\text{propagation}}^{\text{dB}} + L_{\text{through}}^{\text{dB}} + L_{\text{drop}}^{\text{dB}} + L_{\text{crossing}}^{\text{dB}}
\]  

\( L_{\text{propagation}} \) (in dB) is obtained from the intrinsic propagation losses of the optical signal in the waveguide \( P_{\text{propagation}} \) (in dB/cm) and from the waveguide length from source to destination \( l_{s-d} \) (in cm). As for the case of worst-case loss, \( l_{s-d} \) is the longest distance (denoted as \( l_{\text{max}} \)) between the source and destination by considering a serpentine layout. Under the circumstance of only C direction for the signal propagation in a network including \( N \times M \) ONIs, \( l_{\text{max}} \) is defined as following:

\[
\begin{align*}
 l_{\text{max}} &= (N \times M - 2) \times d + (N + M - 2) \times d && M: \text{odd}; \\
 l_{\text{max}} &= (N \times M - 2) \times d + (M - 1) \times d && M: \text{even},
\end{align*}
\]  

where \( d \) is the distance between two neighboring ONIs.

By considering C-CC (i.e., C and CC directions for signal propagation through the use of separated waveguides), \( l_{\text{max}} \) is defined as following:
\begin{align*}
    l_{\text{max}} = & \left\lfloor \frac{(N \times M)}{2} \right\rfloor - 1 \times d + (N + M - 2) \times d & M: \text{odd}; \\
    l_{\text{max}} = & \left\lfloor \frac{(N \times M)}{2} \right\rfloor - 1 \times d + (M - 1) \times d & M: \text{even}.
\end{align*}

\(L_{\text{through}}\) (in dB) is the product result between the loss for each MR in through mode \(P_{\text{through}}\) (in dB) and \(N_{\text{through}}\), the maximum number of MRs in the through mode passed by an optical signal at the corresponding wavelength. By considering the C direction, \(N_{\text{through}}\) equals \((N \times M - 2)\). By considering C-CC directions, \(N_{\text{through}}\) equals \(\left\lfloor (N \times M) / 2 \right\rfloor\) or \((N \times M - 1 - \left\lfloor (N \times M) / 2 \right\rfloor)\) when \(M\) is odd or even, respectively.

\(L_{\text{drop}}\) (in dB) corresponds to the drop loss (i.e., \(P_{\text{drop}}\) in dB) occurring when MRs (i.e., number is \(N_{\text{drop}}\)) are in the ON state. In CHAMELEON, an optical signal crosses only one MR in drop mode during the propagation from the source to the destination. This drop operation occurs in the destination ONI to eject a signal from the waveguide, the loss of which is equal to \(P_{\text{drop}} \times N_{\text{drop}}\).

\(L_{\text{crossing}}\) (in dB) represents the loss due to waveguide crossings (i.e., \(P_{\text{crossing}}\) in dB). The crossing loss can be calculated from \(P_{\text{crossing}} \times N_{\text{crossing}}\), where \(N_{\text{crossing}}\) denotes the number of waveguide crossings. In CHAMELEON, due to the topology and layout properties [1], no waveguide crossing exists.

It is worth noticing that \(l_{\text{max}}\) and \(N_{\text{through}}\) are significantly reduced in the case of the C-CC compared to the C case. This will result in a lower worst-case loss, which directly contributes to the improvement of network energy efficiency. Indeed, for a given receiver sensitivity at a target BER, a lower worst-case loss in the communication path results in a lower minimum required laser output power.

### 5.5. Results

We compare CHAMELEON with Snake [5], ORNoC [1] and SWMR (Single Write Multiple Read), which is modelled on ATAC [5]. Snake and ORNoC are passive networks relying on multistage and ring topologies respectively. ORNoC is evaluated for both C-only and C-CC directions (i.e., ORNoC\(_C\) and ORNoC\(_{C-CC}\)), to take advantage of the combination of signal propagation directions. For CHAMELEON, we also consider two cases: CHAMELEON\(_C\) and CHAMELEON\(_{C-CC}\).
5.5.1. Architectures

The comparison is achieved by considering 3 architectures:

Arch$_1$ is extracted from [5] and is a processor to memory application. Figure 76-a illustrates the layout considered for Snake: it is adapted from [5] to match the requirements of a fully-integrated system in which 4 processors (i.e., P$_0$, P$_1$, P$_2$, P$_3$) and 4 memories (i.e., M$_0$, M$_1$, M$_2$, M$_3$) share the same 20×10mm$^2$ electrical layer. Processors are interconnected through a crossbar located in the center (not shown in the figure), which avoids placing Snake in this area. We assume a 5mm distance $d$ between optical interfaces in the optical network. The layouts for ORNoC and CHAMELEON involve closed waveguides successively crossing M$_0$, M$_1$, P$_1$, P$_3$, M$_3$, M$_2$, P$_2$ and P$_0$ (as shown in Figure 76-b). For a fair comparison with CHAMELEON, we assume that on-chip lasers are also used in Snake.

![Figure 76: Considered Arch$_1$ layout for a) Snake [5] and b) CHAMELEON$_{CC}$.](image)

Arch$_2$ corresponds to 4×4 IP cores (i.e., IP$_0$, …, IP$_{15}$) connected with the optical network (as illustrated in Chapter 3). A 20x20mm$^2$ die size is assumed and $d=5$mm. Figure 77 represents the layout for Snake which is designed to avoid any waveguide crossing between the network interfaces and the Snake multistage itself. Snake is located in the middle of the optical layer for layout optimization purposes and is represented as a box for the sake of clarity. Snake interconnects 16 inputs (in red lines) with 16 outputs (in black lines) through 112 PSEs. The initial structure of Snake would assume 120 PSEs. However, for a fair comparison, we adapt the reduction method from [4] to Snake, in order to remove unused PSEs and reduce the losses. The layout we assume for CHAMELEON and ORNoC is the one illustrated in Chapter 3.
Arch\textsubscript{3} extends Arch\textsubscript{2} to 8x8 IP cores, thus matching the ATAC architecture: 20×20mm\textsuperscript{2} die size and \(d=2.5\)mm are assumed. The size of Snake is increased to match the new connectivity requirement, and the layouts of CHAMELEON and ORNoC are extended from Arch\textsubscript{2}.

Table 10: Injection Loss parameters

<table>
<thead>
<tr>
<th>Optical loss</th>
<th>Conservative (Co)</th>
<th>Aggressive (Ag)</th>
<th>Realistic (Re)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(P_{\text{propagation}})</td>
<td>1.5 dB/cm [5]</td>
<td>0.2 dB/cm [5]</td>
<td>0.5 dB/cm [7]</td>
</tr>
<tr>
<td>(P_{\text{drop}})</td>
<td>0.013 dB [5]</td>
<td>1 dB [5]</td>
<td>0.96 dB</td>
</tr>
<tr>
<td>(P_{\text{through}})</td>
<td>0.05 dB [7]</td>
<td>0.01 dB [5]</td>
<td>0.17 dB</td>
</tr>
<tr>
<td>(P_{\text{crossing}})</td>
<td>0.52 dB [5]</td>
<td>0.05 dB [7]</td>
<td>0.05 [7]</td>
</tr>
</tbody>
</table>

Table 10 summarizes the parameters we used to compare the networks. Similarly to [5], we consider conservative (Co) and aggressive (Ag) values, besides the realistic values (Re) from Chapter 4. Regarding the set of values from “Re”, \(P_{\text{drop}}\) and \(P_{\text{through}}\) are obtained based on the considered MR transmission curves in Chapter 4.

5.5.2. Network Comparisons

We evaluate the following ONoC characteristics: worst-case optical loss (\(L_{\text{WC}}\)) considering both Ag and Co values, number of waveguides (\(N_{\text{WG}}\)), number of wavelengths per waveguide (\(N_{\text{WL}}\)), number of on-chip lasers (\(N_{\text{laser}}\)), and number of MRs (\(N_{\text{MR}}\)). Note that, for Snake, the
number of MRs takes into account both the MRs based filters in the receiver part of the network interface and the MRs based PSEs in the network itself - one PSE counts for 2 MRs.

Regarding *Arch_1*, we estimate the worst-case distance for Snake as following: from P_2 to M_2, the signal will propagate through a distance estimated to be equivalent to 4 times the minimum distance between ONIs (i.e., *d*). Since this worst-case path also suffers from 6 waveguide crossings (4 through the PSEs), the total loss is estimated to be 1.7dB and 6.133dB for Ag and Co values, respectively (considering multi-layer silicon deposited technology, which allows 3D photonic devices, would contribute to reducing the losses [7]). Snake is composed of 56 MRs, including 12 PSEs (as indicated in the bracket in Table 11). It requires 4 wavelengths per waveguide, which is the limit considered for ORNoCs and CHAMELEONS. ORNoC_C shares similar characteristics to Snake when considering conservative values. However, because ORNoC does not suffer from any waveguide crossings, a significant improvement is obtained when considering aggressive values (1.7dB and 0.7dB for Snake and ORNoC_C respectively). Further improvements are obtained for ORNoC_C-CC since the CC direction for signal propagation allows the waveguide length to be reduced from 35mm to 20mm. CHAMELEON directly inherits from the main features of ORNoC: no waveguide crossings, and the possibility to combine C and CC directions. Both features allow the number of waveguides to be reduced from 4 (in CHAMELEON_C) to 2 (in CHAMELEON_C-CC) and the number of on-chip lasers from 128 to 64, respectively. The extra MRs located in the receiver part of the ONIs introduce through losses (i.e., 0.03dB) in the worst-case path for CHAMELEON_C-CC. The overhead in the number of on-chip lasers in CHAMELEON is due to its re-configurability property. Indeed, the complexity of CHAMELEON (e.g., number of lasers) is defined in order to allow the same connectivity in Snake and ORNoC to be configured for the considered example architecture. Moreover, CHAMELEON can open/close communication channels at run-time. This allows, for instance, additional bandwidth to be allocated for a given memory to processor channel by closing other channels. As another example, new channels can be opened between 2 processors, which is impossible for Snake and ORNoC unless it is specified at design time. Since unused lasers are turned-off, CHAMELEON does not suffer from extra power consumption. As a primary conclusion, CHAMELEON offers a run-time flexibility to adapt the bandwidth distribution, according to the connectivity requirements at the price of acceptable extra losses compared to ORNoC (the best solution mentioned in [5]).
Table 11: Comparisons of CHAMELEON with related ONoCs

<table>
<thead>
<tr>
<th>Arch.</th>
<th>Snake</th>
<th>ORNoC</th>
<th>ORNoC,CC</th>
<th>CHAMELEON</th>
<th>CHAMELEON,CC</th>
</tr>
</thead>
<tbody>
<tr>
<td>N_laser</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>128</td>
<td>64</td>
</tr>
<tr>
<td>N_WL</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>N_WG</td>
<td>56 (12)</td>
<td>32</td>
<td>32</td>
<td>128</td>
<td>64</td>
</tr>
<tr>
<td>L_wc Ag</td>
<td>1.7</td>
<td>0.7</td>
<td>0.4</td>
<td>0.76</td>
<td>0.43</td>
</tr>
<tr>
<td>L_wc Co</td>
<td>6.133</td>
<td>5.25</td>
<td>3</td>
<td>5.55</td>
<td>3.15</td>
</tr>
<tr>
<td>Arch.2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N_laser</td>
<td>240</td>
<td>240</td>
<td>240</td>
<td>1,920</td>
<td>960</td>
</tr>
<tr>
<td>N_WL</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>N_WG</td>
<td>16</td>
<td>8</td>
<td>4</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>N_MR</td>
<td>464 (112)</td>
<td>240</td>
<td>240</td>
<td>1,920</td>
<td>960</td>
</tr>
<tr>
<td>L_wc Ag</td>
<td>2.9</td>
<td>1.7</td>
<td>1</td>
<td>1.84</td>
<td>1.07</td>
</tr>
<tr>
<td>L_wc Co</td>
<td>16.8</td>
<td>12.75</td>
<td>7.5</td>
<td>13.45</td>
<td>7.85</td>
</tr>
<tr>
<td>Arch.3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N_laser</td>
<td>4,032</td>
<td>4,032</td>
<td>4,032</td>
<td>129,024</td>
<td>64,512</td>
</tr>
<tr>
<td>N_WL</td>
<td>63</td>
<td>63</td>
<td>63</td>
<td>63</td>
<td>63</td>
</tr>
<tr>
<td>N_WG</td>
<td>64</td>
<td>32</td>
<td>16</td>
<td>32</td>
<td>16</td>
</tr>
<tr>
<td>N_MR</td>
<td>8,000 (1,984)</td>
<td>4,032</td>
<td>4,032</td>
<td>129,024</td>
<td>64,512</td>
</tr>
<tr>
<td>L_wc Ag</td>
<td>5.5</td>
<td>3.45</td>
<td>1.9</td>
<td>4.07</td>
<td>2.21</td>
</tr>
<tr>
<td>L_wc Co</td>
<td>43.26</td>
<td>25.875</td>
<td>14.25</td>
<td>28.975</td>
<td>15.8</td>
</tr>
</tbody>
</table>

Arch2: Snake and ORNoC are crossbars. CHAMELEON basically follows the same trend: close to ORNoC but with more flexibility. By assuming 1GHz modulation speed for the lasers, CHAMELEON offers the same bandwidth as ORNoC and Snake (which can be estimated at 240 Gb/s, i.e., 240×1Gb/s) when configured as a crossbar allocating one wavelength per channel between IP cores. However, if we consider the execution of a streaming application where data propagate from an IP to another, CHAMELEON has the potential to deliver a bandwidth of 1.92 Tb/s by turning on all the laser sources.

Arch3 highlights the resources overhead of CHAMELEON when designed to allow the configuration of a full crossbar between 64 IP cores. For such a large-scale system, permanent connectivity between all the IP cores may not always be required, which could justify a reduction of the number of lasers in CHAMELEON and, therefore, a reduction of its flexibility. Design tradeoffs thus need to be explored by simulating the execution of representative benchmarks.
SWMR only requires 64 off-chip lasers to implement a broadcast, which may lead to less efficient energy/bit transmission. Finally, for Co values, worst-case loss for SWMR is 16.06dB compared to 14.25dB and 15.8dB for ORNoC-C-CC and CHAMELEON-C-CC, respectively.

5.5.3. **Power Efficiency of CHAMELEON**

We evaluate the minimum laser output power required for the evaluated worst-case loss in Arch3 under the target $10^{-12}$ BER [7]. Since we consider a germanium photodetector with the responsivity of 1A/W, the minimum received power is consequently -20dBm (10µW) for error-free operation with the target BER [7]. The results are evaluated for Co, Ag, and Re values from Table 10. Figure 78 represents the estimation for the realistic values. Due to the property of the bi-directional communication, CHAMELEON-C-CC is much more energy efficient. For instance, CHAMELEON and CHAMELEON-C-CC exhibit 1.29mW and 0.16mW for the Re values separately. Compared to CHAMELEON, CHAMELEON-C-CC reduces 95%, 35%, and 88% laser output power for Co, Ag, and Re, respectively. However, simulations are required to evaluate its run-time behavior since, on one hand, we assumed the network already configured as a crossbar (thus not considering the reconfiguration time) and, on the other hand, we do not take advantage of the potential of CHAMELEON to reduce the system power or to improve the execution performances by adapting the bandwidth to the application traffics.

![Figure 78: Power efficiency of CHAMELEON.](image)

5.6. **Discussion**

In CHAMELEON, the channels can be reconfigured at run time and design time. Indeed, the two configuration methods can be combined to use together at the same time, even though they
are presented separately in this chapter. For instance, in each ONI, 8 wavelengths are available in total to receive or to emit optical signal. If the communication requirement for both methods is equal, half of wavelengths can be reserved and arranged for design-time configuration, while the remaining wavelengths may be employed for run-time reconfiguration. In addition, according to the requirement, it is possible to distribute the wavelength resources for design-time or run-time reconfiguration accordingly.

In the proposed network, the laser output power is evaluated according to the worst-case loss among all the optical paths and it is provided equally for the communications. The energy efficiency is improved by employing the combination of C and CC directions in different waveguides. Moreover, on-chip lasers can be turned off if not used, to reduce the laser power consumption. To further ameliorate the energy efficiency, the laser output power can be offered correspondingly according to the different losses along the optical paths.

In addition, thermal variation may have an influence on the communication quality. Since on-chip lasers are utilized in the interfaces to emit optical signal, it is necessary to take into account the influence of temperature variation on the lasers. Therefore, the thermal-aware tuning approach in the previous chapter can be adapted and applied to this architecture, in order to reach a trade-off between the BER and power consumption. The adapted tuning method needs to consider in two cases for CHAMELEON: design-time and run-time. Regarding design-time case, the transmission model and power model are fixed once the configuration is determined. For run-time configuration, it is necessary to update both models on line according to the established communication channels. This requires run-time calibration process to explore the tuning power options for the lasers and MRs.

5.7. Conclusion

In this chapter, we proposed a reconfigurable channel efficient optical network on chip, named CHAMELEON. To the best of our knowledge, this network is the first allowing the run-time creation of point-to-point (i.e., dedicated) channels without any waveguide crossing in the optical path, which leads to energy-efficient optical transmission of data. Compared to related static (i.e., non-configurable) ONoCs designed to fully interconnect 8x8 cores, CHAMELEON can be configured at run-time to realize the same connectivity, with an energy overhead of 7.4% when compared to the most energy-efficient non-configurable solution. The ring topology and the
regular interfaces contribute to the good scalability of CHAMELEON. The combined use of clockwise and counter-clockwise directions for signal propagation allows a substantial improvement of its energy-efficiency and scalability. The reconfigurable ability of CHAMELEON allows the bandwidth to be adapted between IP cores according to application traffic requirements, which will further reduce the energy/bit transmission of data for a given application. Furthermore, CHAMELEON can be considered to adapt for interconnects in datacenters.

5.8. References


Chapter 6. Conclusion and future work

6.1. Conclusion

Silicon photonic interconnects on chip have the potential to overcome the limitations of traditional electrical interconnects in aspects of communication performance, power efficiency, and hardware cost. However, due to the current technology limitations, it still faces challenges since it requires heterogeneous integration of materials (e.g., silicon, silica, Ge, etc.), functions (e.g., processor, memory, communication network, etc.), and domains (e.g., electronics and photonics). In this thesis, we investigate energy efficiency improvement from three aspects: topologies/layouts, thermal variation, and architecture.

6.1.1. Topologies/layouts

From the point view of topology and physical layout, we explore several topologies and compare their implementations using single-layer and multi-layer technologies. Matrix, λ-router, Snake, and ring have been considered. The number of lasers, MRs, photodetectors, and wavelengths, are estimated according to the network size. The results show that ORNoC in the ring topology avoids the use of MRs in optical interconnects, leading to a lower optical loss. The limitation in the number of wavelengths can be alleviated by adding extra waveguides.

The physical layouts of the topologies are proposed and compared. For Matrix, λ-router and Snake, two new layouts are proposed. The first type avoids any waveguide crossing (named as layout\textsubscript{w\textsubscript{sl}X}), and the second type reduces the worst-case waveguide length between IP cores (named as layout\textsubscript{wX}). For ring topology, serpentine layouts are considered for both unidirectional and bidirectional implementations of ORNoC: ORNoC\textsubscript{C} and ORNoC\textsubscript{C-CC}. Worst-case loss (L\textsubscript{WC}) and average loss (L\textsubscript{avg}) are used for the comparison. L\textsubscript{WC} gives the minimum laser output power per wavelength and L\textsubscript{avg} indicates the potential improvement of total laser output power in the optical interconnects. We first evaluate all the layouts under different number of IP cores for a given die size. Results show that ring-based networks can facilitate the implementation characterized by lower worst-case and average optical losses, leading to the most power-efficient solution. Moreover, for a given number of IP cores (e.g., 6x6) under different realistic die size, ring-based networks also show lower worst-case optical losses, outperforming other three layouts.
We further explore the design space by considering different technological parameters (e.g., the optical propagation loss and waveguide crossing loss parameters) under various die sizes for a given number of IP cores. It is shown that ring-based topology implementations exhibit higher power efficiency compared to matrix-based (i.e., Matrix topology) and multistage-based (i.e., \( \lambda \)-router and Snake topologies) network implementations.

Besides the single-layer layout implementations, we also evaluate the corresponding multi-layer layout implementations of different topologies by considering the multi-layer deposited silicon technology. Similar to the single-layer layout implementations, for Matrix, \( \lambda \)-router and Snake topologies, two multi-layer layouts are proposed including one with minimized waveguide length (i.e., \( \text{layout}^{\text{wX}} \)) and the other without waveguide crossing (i.e., \( \text{layout}^{\text{woX}} \)). For ORNoC in ring topology, a multi-layer layout implementation (ORNoC\( _{\text{ML}} \)) is only proposed for ORNoC\( _{\text{C}-\text{CC}} \) since it presents lower optical loss compared to ORNoC\( _{\text{C}} \). In the meanwhile, we propose a design method to allocate communications on optical paths exhibiting the lowest losses, taking into consideration the two layers. The results show that the multi-layer implementation can achieve a big improvement in optical loss compared with the single-layer implementation. For different number of IP cores, both worst-case loss and average loss are reduced in multi-layer implementations. Results show that, to interconnect 8x8 cores, the multi-layer implementations lead to a reduction of 42% and 46% on average in the worst-case and average optical losses, respectively. Especially, this reduction is bigger for those layouts which exhibit more waveguide crossings in the single-layer implementation. For instance, for the 8x8 size of Matrix\( ^{\text{wX}} \), the reduction of the worst-case loss can reach up to 69%. This result indicates that multi-layer implementation is promising to be applied to those layouts with more waveguide crossings. The reduction of optical loss has an immediate impact on the required laser output power, which can decrease up to 85%, thus contributing to a higher energy efficiency of the optical network. We evaluate \( L_{\text{WC}} \) and \( L_{\text{avg}} \) under different number of IP cores. Ring-based topology still exhibits lower worst-case and average losses compared to other topologies. The similar conclusion can be observed for a given number of IP cores under different die sizes. The ring is the most energy-efficient topology among all studied architectures. On average, it leads to 66% reduction of worst-case loss when compared to the other three topologies. We also investigate the impact of different technological parameters on the energy efficiency of Matrix\( ^{\text{wX}} \) and ORNoC\( _{\text{ML}} \). This
allows us selecting the proper topology to be used for a given technological platform and identifying the constraints on technological parameters for a given topology.

6.1.2. **Thermal variation**

Because of the uneven distribution of power consumption over the chip, temperature gradient may exist in silicon photonic interconnects. This variation has a negative impact on the communication reliability and energy efficiency. Based on our analysis of the influence of the thermal variation, we propose a methodology to design thermal-robust silicon photonic interconnect.

The methodology allows exploration of the design space at both device level and system level. For this purpose, the main characteristics of the optical devices (e.g., lasers, MRs, waveguides, photodetectors) are taken into account in device-level models. Architectural aspects such as interconnect size and topology/layout are taken into account in system-level models. From a given chip activity, thermal simulation allows the estimation of temperature profiles in the chip and analytical models allow calculation of the tuning power consumption and BER. Design space exploration can then be carried out to optimize energy efficiency and reliability of the optical interconnects.

We further propose a thermal-aware on-chip laser tuning method to overcome the wavelength variation induced by the temperature variation, while achieving targeted BER at the same time. This method is mainly dependent on the tuning of the laser driver current. As a result, it tunes both laser wavelength and MR resonant wavelengths along one communication channel, instead of tuning only MR resonant wavelengths in the conventional method. Furthermore, in order to estimate the effectiveness of the proposed method, we set up a transmission model and a power model to evaluate the reliability and energy efficiency respectively in the simulation model we established. In these models we also take the thermal sensitivity of the on-chip laser sources into account. The evaluations are carried out by taking the MWSR communication scheme as an illustrative application of the method in a 3D stacked architecture which interconnects multiple processors. Using the thermal simulator, we can obtain the detailed temperature maps over the whole chip. In the simulations, we utilize different chip activities to explore a better tradeoff between reliability (e.g., BER) and energy efficiency. Through this exploration, we propose strategies to minimize either the energy consumption or the BER. We
explore to improve the energy efficiency by using an on-chip laser with higher efficiency, therefore reducing the impact of thermal variation. From the simulation results, we can achieve the conclusion that the proposed method which combines the tuning of lasers and MRs has significant advantages on tuning power than the conventional method which only tunes MRs, when the uniform chip activity decreases.

6.1.3. **Architecture**

To make use of the good properties from the exploration of topologies and layouts, we propose CHAMELEON based on ring topology, utilizing both clockwise (C) and counter-clockwise (CC) communication directions. In CHAMELEON architecture, the interfaces are the kernel components, which enable reconfiguring the communication channels as MWSR, SWMR, MWMR, and SWSR at either design time or run time. Through the reconfiguration of interfaces, different communication schemes can be implemented. In this thesis, we describe the schemes for design-time configuration and run-time configuration: i) by application mapping and ii) by communication protocol. For the design-time configuration, we use the MP3 audio decoder application to illustrate the configuration process. For the run-time configuration scheme, we propose a communication protocol and a resource allocation algorithm. To evaluate the proposed architecture, we use the optical loss model and the minimum laser output power metric. We compare the proposed architecture with three architectures for $2 \times 2$, $4 \times 4$, and $8 \times 8$ cores. Compared to passive ONoCs, CHAMELEON configured to implement the same connectivity leads to 7.4% energy overhead. Moreover, the combined use of clockwise and counter-clockwise directions for signal propagation in CHAMELEON allows a substantial improvement of its energy-efficiency and scalability.

In this thesis, we contributed to the energy efficiency improvement of on-chip silicon photonic interconnects. In the following, we summarize perspectives to this work.

6.2. **Future work**

6.2.1. **Thermal-aware laser tuning at run-time**

A major challenge for the practical use of our thermal-aware on-chip laser tuning method at run-time is the calibration process. Indeed, lasers and MRs have to be tuned rapidly in order to ensure the availability of the optical link. The design method we proposed relies on 2D
temperature maps generated through stationary thermal simulation. Working on the run-time calibration process will require transient thermal simulations, which is possible using the IcTherm tool. Existing device models will need to be enriched with timing characteristics such as latency and new models have to be introduced. This run-time calibration process is potential to reach a compromise between the tuning power consumption and BER.

The calibration requires a monitoring of the BER; this can be achieved either i) by sending a predefined data set on the optical channel and estimating the errors, or ii) measuring the intensity of the light received by the photodetector. While the former approach leads to extra latency due to the need to send enough data to measure the BER, it is also probably the most accurate method considering the crosstalk induced by WDM. Processing is then needed to evaluate the state of the optical channel and if necessary to calibrate the optical devices. It will be needed to compare algorithms according to a set of predefined scenario and to select the most suitable option (according to convergence time, optimization results and robustness for instance). Hardware or software implementation of the algorithm will thus be carried out, which will allow estimation of the execution latency to be taken into account into the transient thermal simulation. Parameters such as the MRs/lasers grouping level (which impacts both controller complexity and tuning efficiency) will also be carried out.

Since the proposed calibration process is generic, we will be able to i) compare the tuning efficiency for on-chip and off-chip laser sources and ii) investigate the impact of multi-layer silicon deposited technology on the tuning efficiency.

6.2.2. **Need for a unified MR transmission model**

For many years, system-level models mostly relied on analytical values for MR transmission. More recently, rectangular, Gaussian, and transmission in [1] have been introduced. Their main purpose is to better consider crosstalk and device-related specificities such as the fabrication variability, which comes at a price of longer simulation time. The multiplication of models raises the question of standardized approaches and models to evaluate the interconnects. Hence, it would be interesting to investigate whether a unified MR model could be proposed to the community to allow accurate but slow simulation or fast but less accurate estimation.
6.2.3. **Complementary communication path to reduce laser power**

Evolving on the serpentine-layout pattern, we proposed an energy-efficient communication approach, where we recover the absorbed light (which is discarded in traditional schemes), and then re-inject it in a complementary waveguide to provide differential optical communication. With this approach, it is possible to reduce the input laser power and increase the energy efficiency of the optical communication. Our approach is generic and can be applied to a large panel of existing architectures.

![Complementary communication path to reduce laser power](image)

**Figure 79:** Transmission of data ‘1’ and ‘0’ through primary and complementary paths respectively.

Figure 79-a illustrates our approach using a MWSR-like architecture, assuming 3 Writers, one waveguide and a single wavelength (i.e., one MR per core). In the example, Core₁ communicates with Core₃. Hence, the MRs in Core₀ and Core₂ are turned OFF (i.e., at off-resonance) and the MR in Core₁ is in the modulation state, i.e., it switches from OFF state to ON state (i.e., at resonance) to transmit data ‘1’ and ‘0’ respectively. Note that there are no MRs in the reader structure in Figure 79-a since a single wavelength was considered. The details of the complementary communication can be found in appendix.

However, for the same optical data, the signal transmitted in the complementary path experiences longer distance than the signal in the primary path, which leads to a delayed arrival time of the signal on the complementary path. This could be solved by introducing delay lines on the primary path.
We could also explore the use of Optical Multi-Level Signaling (OMLS) modulation to use multiple levels of amplitude in order to represent multiple encoded data [2][3].

6.3. References


A.1. Approach Overview

A.1.1. Primary Path: Transmission of Data ‘1’

Data ‘1’ leads to a MR in the OFF state to let the light pass through. Similarly to the related approaches, the light propagates through the so-called primary path: it crosses the modulator and continues propagating along the same waveguide until reaching the photodetector, as illustrated by the red arrow in Figure 80-a. The power of the optical signal decreases due to losses from waveguide propagation, crossed modulators and photodetector, as illustrated by the red line in Figure 80-b. The optical power received by the photodetector ($S_{p,1}$) must be high enough to ensure proper detection and photo-electronic conversion through the Trans-Impedance Amplifier (TIA). Conversely, the MR is turned ON for data ‘0’ and diverts most of the light from the primary path, leading to a low optical power $S_{p,0}$ at the photodetector. While the sensitivity of the photodetector (in the order of -20dBm [1]) is a key parameter for energy-efficient optical interconnect, the actual received power is usually higher to distinguish data ‘1’ ($S_{p,1}$) from data ‘0’ ($S_{p,0}$) and to ensure high enough signal-to-noise ratio (SNR) in the worst-case scenario. It is
well known that optical interconnects are sensitive to crosstalk and variations in both the fabrication process and local temperature. We define $S_p$ as the difference between the signal power received when transmitting ‘1’ and ‘0’ in the primary path.

**A.1.2. Complementary Path: Transmission of Data ‘0’**

When the MR is in the ON state to transmit data ‘0’ in the primary path, instead of “absorbing” the light as in related approaches, we propose to drop the light into a secondary path, the so-called complementary path, as illustrated by the blue arrow in Figure 80-a. In this example, it is composed of a waveguide propagating the light towards a second photodetector receiving $S_{c,0}$. This complementary structure allows the differential transmission of the data, which contributes to increasing the detected signal power and ultimately reduces the laser power consumption. The signal propagating in the complementary path experiences some power increase due to the crosstalk signals dropped from the primary path (i.e. dotted line arrows from Core$_0$ and Core$_2$ in the figure). This positive effect is partially counteracted by the increase of $S_{c,1}$, the crosstalk level in the complementary path when a ‘1’ is transmitted (i.e. dashed red line), as illustrated in Figure 80-c. $S_c$ is the difference between the signal power received in the complementary path when transmitting ‘0’ and ‘1’. This additional received power enables the value of the transmitted data to be better distinguished thanks to a higher dynamic of the signals. Getting $S_p + S_c$ instead of $S_p$, it is thus possible to reduce the input laser power by a factor of $S_p/(S_p+S_c)$, i.e. with an energy efficiency gain of $S_c/(S_p+S_c)$.

**A.1.3. Micro-Architecture of the Receiver**

The addition of a complementary path to the conventional transmission structure creates the need for a modified receiver, which will benefit from the differential transmission to improve the optical signal quality and allow working at lower laser input power. To do so, the photocurrents provided by the photodiodes on the primary and complementary paths are substracted by a simple series connection of the photodiodes between supply and ground, the difference current being fed to a conventional TIA, as depicted in Figure 80-a.

The analytical models presented hereafter consider a linear conversion from the photocurrents to the TIA output, which actually means the signal is considered to propagate without alteration from the optical subsystem to the electrical subsystem.
A.2. Elemental blocks

Figure 81 illustrates the elemental optical writing and reading structures, respectively named writer $w_j$ and reader $r_j$. In the writer, the modulation of data ‘1’ leads to the propagation of the signal at $\lambda_j$ on the through port (Figure 81-a). The losses of the signal are thus expected to be the same as in traditional architectures. If data ‘0’ is modulated, the signal at $\lambda_j$ is strongly attenuated on the through port and is mainly redirected to the drop port. The signal then i) propagates on a waveguide following the backward-direction and ii) is redirected to the forward-direction using a U-shaped waveguide (Figure 81-b). In order to reduce the waveguide bending losses $L_b$, a $40\mu m$ radius is considered, which leads to $-0.025dB$ losses (Figure 81 is not at the right scale: the radius of the ring is around 1-10µm and is thus smaller than the U-shaped waveguide).

![Diagram of elemental optical writing and reading structures](image)

Figure 81: The writer $w_j$ includes an MR that a) let the signals at $\lambda_j$ continue propagating on the primary path or b) drops the resonating signal toward the complementary path. The reader $r_j$ is symmetric and includes two MRs allowing to a) let signals continue propagating or d) filter them for photodetection.

The aim of $r_j$ is to filter the same wavelength on both primary and complementary paths, as illustrated in Figure 81-c and -d. For this purpose, the traditional reader structure is duplicated and the resulting MR pair is controlled by a common signal. These additional MRs lead to the actual cost of the proposed approach. The reduction of the laser power needs to be compared to the increase of the area.
A.3. Analytical model

A.3.1. General MWMR model

Figure 82: Generic MWMR architecture in which CoreS transmits data to CoreT. The light, generated from CW lasers propagates on the primary path, crosses the writer parts of a first set of cores until reaching CoreS for the modulation. The modulated signals then propagate on primary and complementary paths (data ‘1’ and ‘0’ respectively), cross a second set of writers, a set of readers until reaching the photodetectors of CoreT.

Figure 82 illustrates the MWMR architecture we are considering. It is composed of NW Writers and NR Readers (the general case allows NW ≠ NR). Each waveguide pair of the network (a single pair in the figure) performs 2 round trips to successively cross the Writers and the Readers. CW lasers inject optical power in each primary path. We assume that NWL wavelengths are used to modulate the signal (i.e., λ₀, λ₁, ..., λNWL-1). The modulation of the signals occurs in WS, the Writer part of the source core CoreS (note that WS is composed of w₀, w₁, ..., wNWL-1), and experiences the detection in the RT, the Reader part of the target core CoreT (RT is composed of r₀, r₁, ..., rNWL-1). The aim of the analytical model is to evaluate the laser power reduction achievable with the use of the complementary path. For this purpose, we distinguish the signal transmission in the set of all writers and the set of all receivers.

A.3.1.1. Transmission in the Writers

The losses experienced by the optical signal crossing the writers will depend on i) the modulated data dᵢ (i.e. ‘0’ or ‘1’) and ii) the core position where the modulation takes place, WS. In order to distinguish the transmissions T of a signal at wavelength λⱼ in the primary path and the complementary path, we define \( T_{w,p,wₖ,dⱼ}[j] \) and \( T_{w,c,wₖ,dⱼ}[j] \) respectively. In this notation, \( dⱼ \) is the value of the modulated data (‘0’ or ‘1’) at \( λⱼ \), which is important to take into account since it determines the optical path. These transmissions allow the power level of the optical signal to be
evaluated before entering the set of Readers (in the second waveguide round trip). For the sake of clarity, the formulas for $T_w$ are given in basic transmission models.

### A.3.1.2. Transmission in the Readers

Due to a symmetric micro-architecture and control circuitry of the reader structure, the signals in primary and complementary paths experience the same transmission to reach $R_T$, and are expressed as $T_{r,R_T,j}[j]$. After crossing intermediate Reader cores ($R_0\ldots R_{T-1}$), the signals at wavelength $\lambda_j$ reach $R_T$ where they are dropped by the appropriate filters toward photodetectors. The formula for $T_r$ is also given in basic transmission models.

### A.3.1.3. Received Signal Power

In order to estimate the gain induced by the complementary path, we define $S_{p,w_S,R_T,j,d_j}$ and $S_{c,w_S,R_T,j,d_j}$ as the signals modulated in $W_S$ and received by the $j^{th}$ photodetectors in $R_T$ on primary and complementary paths respectively. The four cases are formally defined as:

\[
S_{p,w_S,R_T,j,0} = T_{w_p,w_S,0}[j] \cdot T_{r,R_T,j}[j] \cdot P_{in}[j] \\
S_{p,w_S,R_T,j,1} = T_{w_p,w_S,1}[j] \cdot T_{r,R_T,j}[j] \cdot P_{in}[j] \\
S_{c,w_S,R_T,j,0} = T_{w_c,w_S,0}[j] \cdot T_{r,R_T,j}[j] \cdot P_{in}[j] \\
S_{c,w_S,R_T,j,1} = T_{w_c,w_S,1}[j] \cdot T_{r,R_T,j}[j] \cdot P_{in}[j]
\]

where $P_{in}[j]$ is the laser power coupled into the waveguide at $\lambda_j$. $S_{p,w_S,R_T,j}$ (resp. $S_{c,w_S,R_T,j}$) corresponds to the difference between the received signal powers for $d_j='1'$ and $d_j='0'$ (resp. ‘0’ and ‘1’). From this, we obtain the signal transmission improvement for communication $W_S \rightarrow R_T$, which is defined as

\[
\frac{S_{c,w_S,R_T,j}}{S_{p,w_S,R_T,j} + S_{c,w_S,R_T,j}}
\]

By considering the worst-case transmission improvement among the possible communication pairs, the laser power reduction is estimated.
For the sake of clarity, the equations described above do not take into account the inter-channel crosstalk (which occurs due to the signals modulated at other wavelengths). We refer to the basic transmission models for the general case in which inter-channel crosstalk is considered.

A.3.1.4. Basic transmission models

In this subsection, we consider communication between Writer \( W_S \) and Receiver \( R_T \). The received signal power on \( r_j \) (i.e., the reader of \( R_T \) at wavelength \( \lambda_j \)) depends on \( d_i \) and \( d_j \), the data modulated at \( \lambda_i \) (received power at \( \lambda_j \) is crosstalk) and \( \lambda_j \) respectively. They are defined by \( s_{p,W_S,R_T,j,d_j} \) and \( s_{c,W_S,R_T,j,d_j} \) which are formalized in equations (6) and (7) respectively.

\[
S_{p,W_S,R_T,j,d_j} = \sum_{i=0}^{N_{w,c}-1} (T_{w,p,W_S,i} \cdot T_{r,R_T,j} \cdot P_{w,i}) \tag{6}
\]

\[
S_{c,W_S,R_T,j,d_j} = \sum_{i=0}^{N_{w,c}-1} (T_{w,c,W_S,i} \cdot T_{r,R_T,j} \cdot P_{w,i}) \tag{7}
\]

They depend on:

- \( T_{w,p,W_S,i}[i] \) (equation (8)), transmission in the primary path of the writer parts, which is the same with that in traditional architectures.
- \( T_{w,c,W_S,i}[i] \) (equation (9)), transmission in the complementary path of the writer parts. It is divided into: i) the transmission before the modulation, ii) the transmission from primary to complementary path where the modulation occurs and iii) the transmission after the modulation.
- \( T_{r,R_T,j}[i] \) (equation (10)), transmission in the reader parts to reach the reading core. The transmission of signals at \( \lambda_i \) across the intermediate Readers and dropped by \( R_T \) is defined.

\[
T_{w,p,W_S,i}[i] = \left[ \left( L_p \right)^{N_{w,c}-1} \left( L_p \right)^{N_{w,c}-1} \prod_{i=0}^{N_{w,c}-1} \phi_{w}(\lambda_i, \lambda_i + \Delta \lambda) \right]^w \left( \prod_{i=0}^{N_{w,c}-1} \phi_{w}(\lambda_i, \lambda_i + d_i \lambda) \right)^w \left( \prod_{i=0}^{N_{w,c}-1} \phi_{w}(\lambda_i, \lambda_i + \Delta \lambda) \right)^w \left( \prod_{i=0}^{N_{w,c}-1} \phi_{w}(\lambda_i, \lambda_i + d_i \lambda) \right)^w \tag{8}
\]
In these equations, $L_p$ is the propagation loss. $l_{w,\text{total}}[i]$ and $l_{r,\text{total}}[i]$ (resp. $N_{w,b}[i]$ and $N_{r,b}[i]$) are the total waveguide length (resp. number of waveguide bends) experienced by signal at $\lambda_i$ in Writers (in primary path) and Readers parts. Regarding the waveguide length experienced by signal at $\lambda_i$ coupled from the primary path into the complementary path, we define it as $l_i[i]$, where $v$ is the considered Writer (i.e., $v=\text{Ws}$ when considering the modulating Writer).

### A.3.2. Depopulated models

This MWMR model allows the gain of our approach to be applied in network architectures such as Flexishare [1]. In addition, the analytical model can be adapted to other types of network such as MWSR, SWMR and SWSR. The MWMR model is adapted based on the implementation of the complementary path structure in these networks, which is illustrated in Figure 83.

Figure 83-a illustrates a MWSR architecture which is obtained by considering a single target core per waveguide. In such network architecture, each core is reachable through a set of dedicated waveguides. Among others, MPNoC [2], Corona [3] and Clos [4] rely on MWSR. On the opposite, SWMR-like architectures (Figure 83-b) imply a single source core per waveguide, i.e. the arbitration occurs in the Readers. Networks such as Firefly [5], LumiNOC [6], ATAC unicast channel [7] implement SWMR. Finally, SWSR-like architecture is obtained by allocating, at design time, dedicated wavelengths, i.e. no arbitration is required. The immediate implementation of a SWSR network leads to a single writing core and a single reading core per waveguide. It thus implies dedicated waveguides for Core_0 $\rightarrow$ Core_1, Core_0 $\rightarrow$ Core_2, Core_1 $\rightarrow$ Core_0,
etc. as illustrated in Figure 83-c. For all these scenarios (Figure 83-a-b-c), we have derived the analytical model from the Section A.3.1.4, taking into account the (possibly different) number of Writers (x) and Readers (y), i.e. which is denoted as xWyR.

![Diagram](image)

**Figure 83.** Implementation of the complementary path structure in ring-based a) MWSR, b) SWMR and c) SWSR like networks. Part d) illustrates its implementation on sectioned waveguides based networks.

Our approach suits well with serpentine layout-based networks since it does not add complexity in the layout and does not introduce waveguide crossing. Hence, it can also be applied to networks relying on sectioned waveguides (Figure 83-d) such as ORNoC [8] and SUOR [9]. The improvement evaluation of the complementary path in these networks is remained as future work. While it could also be applied to other topologies such as Mesh, Torus [10] and Multi-Stage, it would need to duplicate all rings used as routers, and would also introduce many waveguide crossings that will, in turn, reduce the signal power on primary and complementary paths. For this reason, these topologies options are not considered.

**A.4. References**


List of publications

Journal papers and Book Chapters


International conference papers


(invited) Workshop papers and invited conference papers


**Under Submission paper**

AUTORISATION DE SOUTENANCE

Vu les dispositions de l'arrêté du 7 août 2006,

Vu la demande du Directeur de Thèse

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Ecole doctorale ELECTRONIQUE, ELECTROTECHNIQUE, AUTOMATIQUE

Fait à Ecully, le 7 décembre 2016

P/Le directeur de l'E.C.L.
Le directrice des Études

M-A. GALLAND
Attestation de réussite du Doctorat de l’Université de LYON opéré au sein de l’Ecole centrale de Lyon

Le directeur de l'Ecole centrale de Lyon soussigné certifie que :
Madame LI Hui
Née le 6 mars 1988 à Shanghai (Chine)

a obtenu le grade de docteur dans son établissement,

**Ecole Doctorale** N° ED 160 : ELECTRONIQUE, ELECTROTECHNIQUE, AUTOMATIQUE
**Spécialité de doctorat** : Electronique, micro et nanoélectronique, optique et laser

**Titre de la thèse** : Design Methods for Energy-Efficient Silicon Photonic Interconnects on Chip
soutenue publiquement à l'Ecole centrale de Lyon, le 9 décembre 2016

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Fait à Ecully, le 4 janvier 2017

Pour le Directeur de Ecole centrale de Lyon
La Directrice des Etudes

[Signature]

Marie-Annick GALLAND